

HSF Property: ROHS or Halogen-Free(5L3?)

LOUIS1.1

DB BUILD : VRAM x4 pcs

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2011.09.21

STACK UP

LAYER	NAME	HIGH SPEED
L1	TOP	HIGH SPEED
L2	GND	
L3	IN1	HIGH SPEED
L4	VCC	
L5	IN2	
L6	IN3	HIGH SPEED
L7	GND	
L8	BOT	HIGH SPEED

XX BUILD: VRAM x 4pcs

SAMSUNG-Main Board: 1310AXXXXXXXX (3D)
HYNIX-Main Board: 1310A2489901 (3D)

SAMSUNG-Main Board: 1310AXXXXXXXX (2D)
HYNIX-Main Board: 1310A2489902 (2D)

UMA-Main Board: 1310A2489903

MB PCB Board's IEC PN: 6050A2489901

SM BUS address / I2C

Cypress: 0xE0, 0x40
Audio amp: 0xC0
G-Sensor: 0x30, 0x32, 0x38, 0x3A
P-Sensor: 0x20, 0x21, 0x22, 0x23, 0xB0, 0xB1, 0xB2
DGPU Thermal: 0x82
Thermal IC: 0x98, 0x9A
Battery: 0x16
Charger IC: 0x12

21-OCT-2002		
DATE	CHANGE NO.	REV.

DRAWN	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					MODEL, PROJECT, FUNCTION			
CHECK					Everest Main Board			
RESPONSIBLE								
SHEET					SIZE	CODE	DOC NUMBER	REV
FILE NAME:					C	CS	1310xxxxx-0-0	X01
PN	xxx				SHEET			

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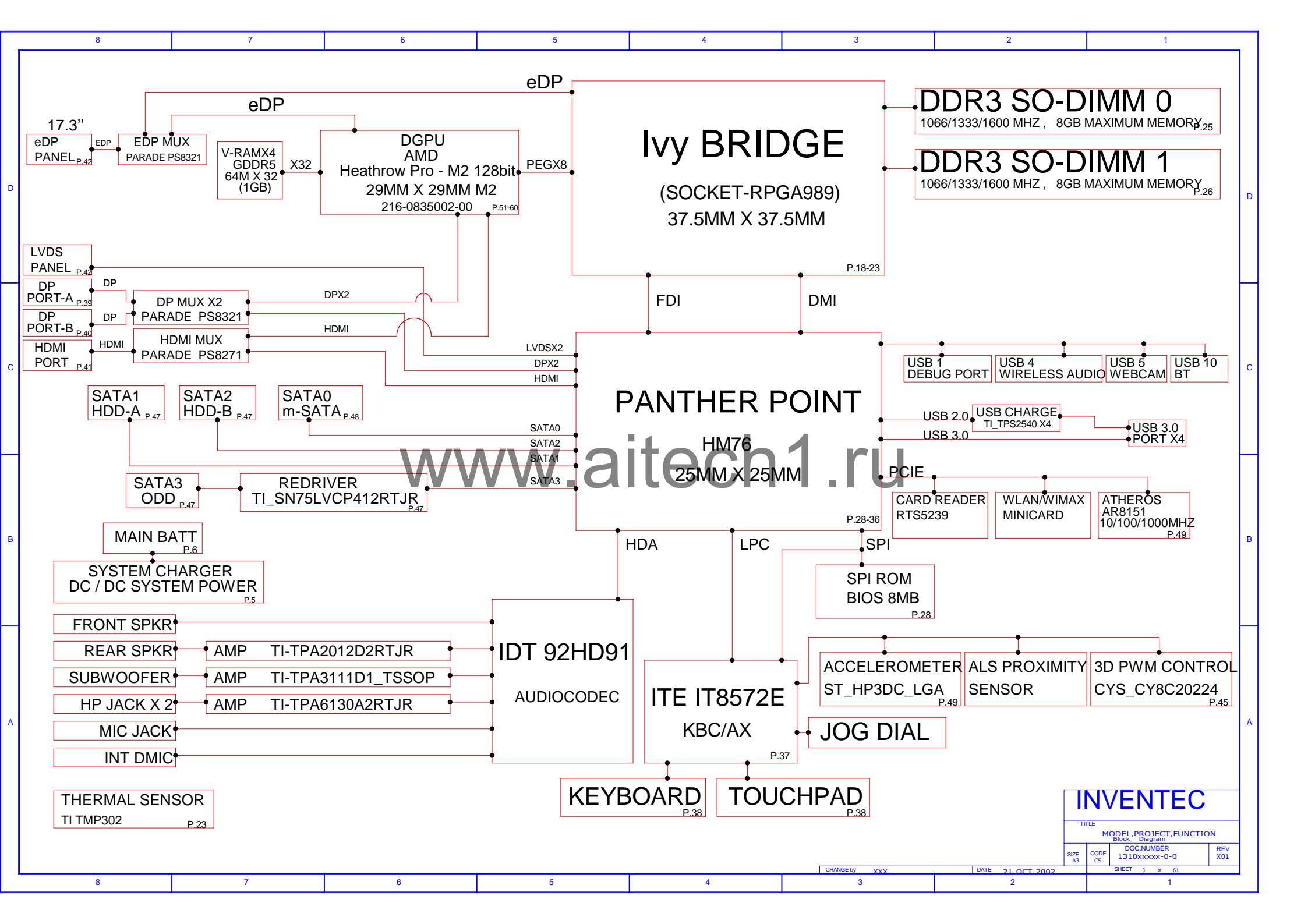
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03. Block Diagram
04. Power Procedure
05. Charger
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07. P3V3A &P5V0A
08. P1V5
09. +VTT
10. P1V8
11. PVSA
12. PVCORE - 1
13. PVCORE - 2
14. PDGPU
15. PVDDCI & PVPCIE
16. EN PORT
17. P5V0S & P3V3S & P1V5S
18. CPU-1
19. CPU-2
20. CPU-3
21. CPU-4
22. CPU-5
23. CPU-6
24. Fan
25. DDR3-DIMM0
26. DDR3-DIMM1
27. USB30_REDRIIVER
28. PCH-1
29. PCH-2
30. PCH-3
31. PCH-4

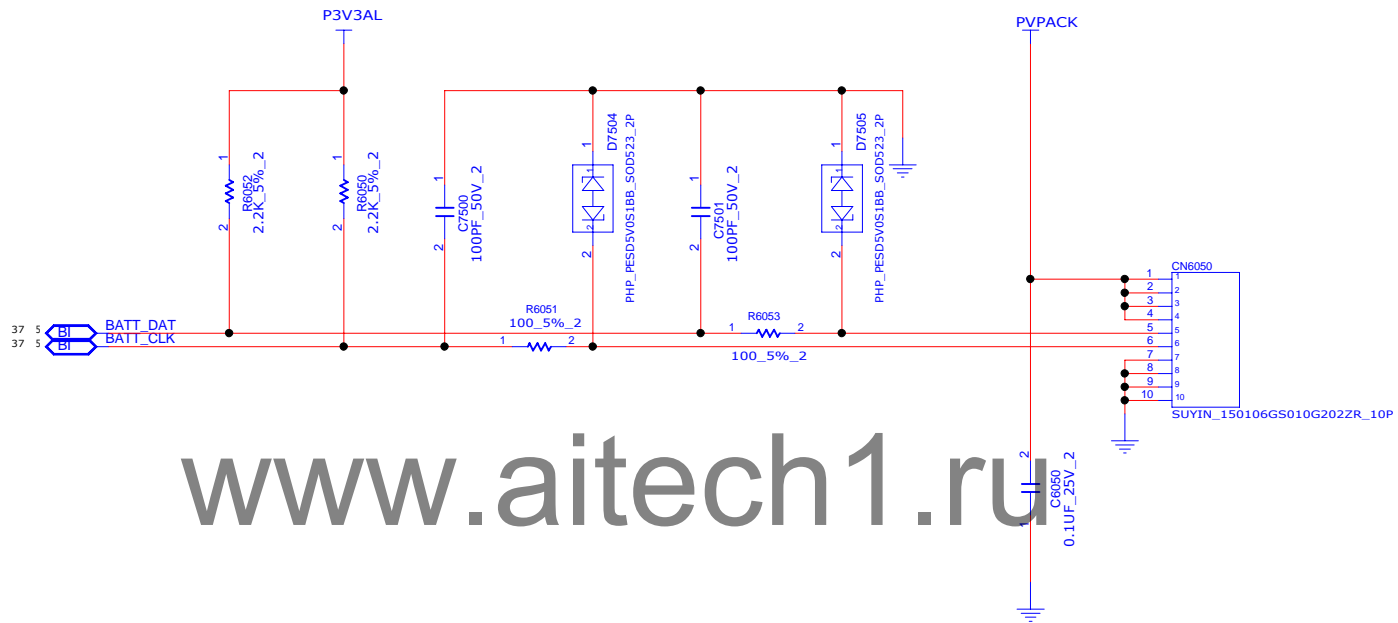
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59. VRAM-1
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INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
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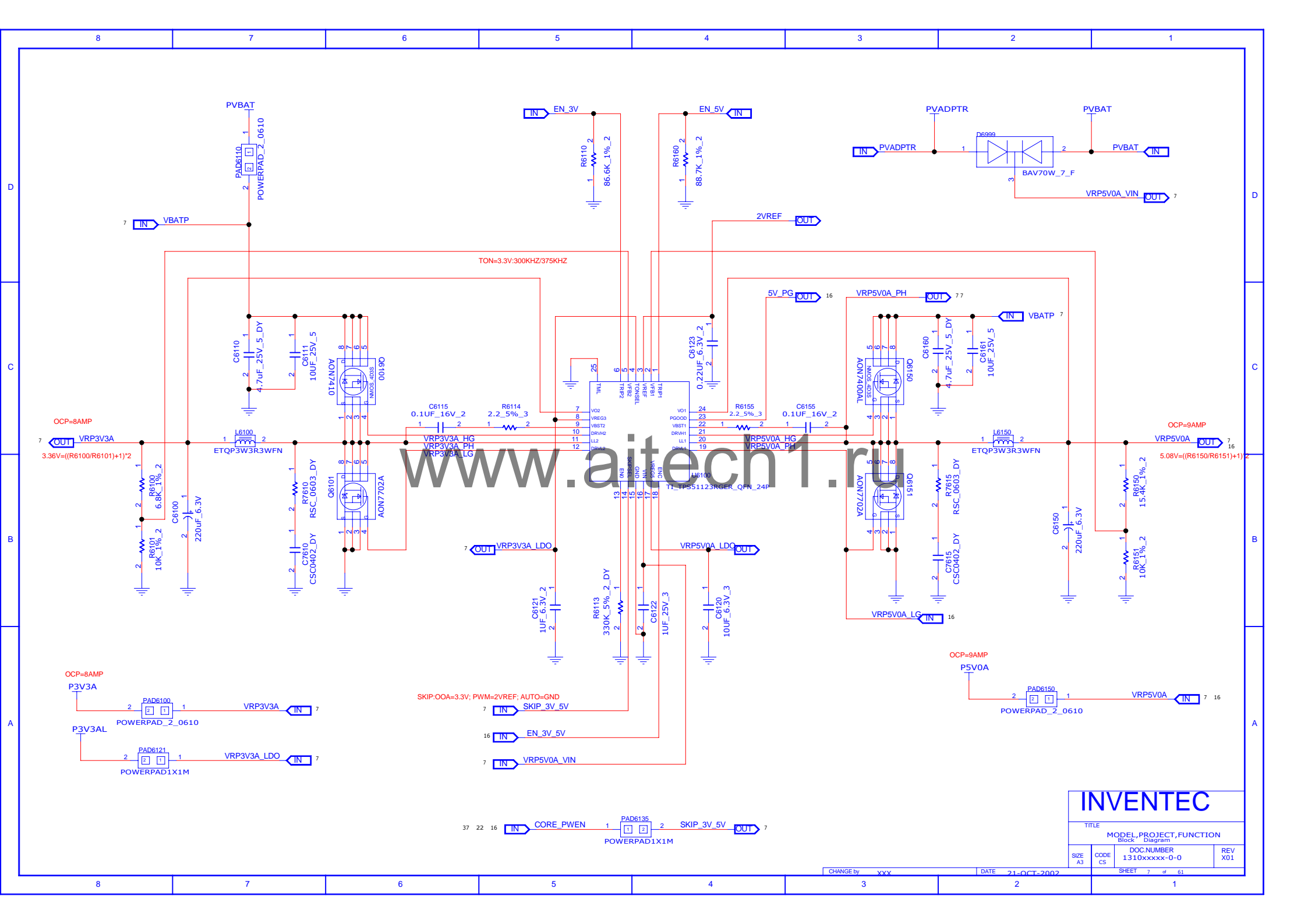
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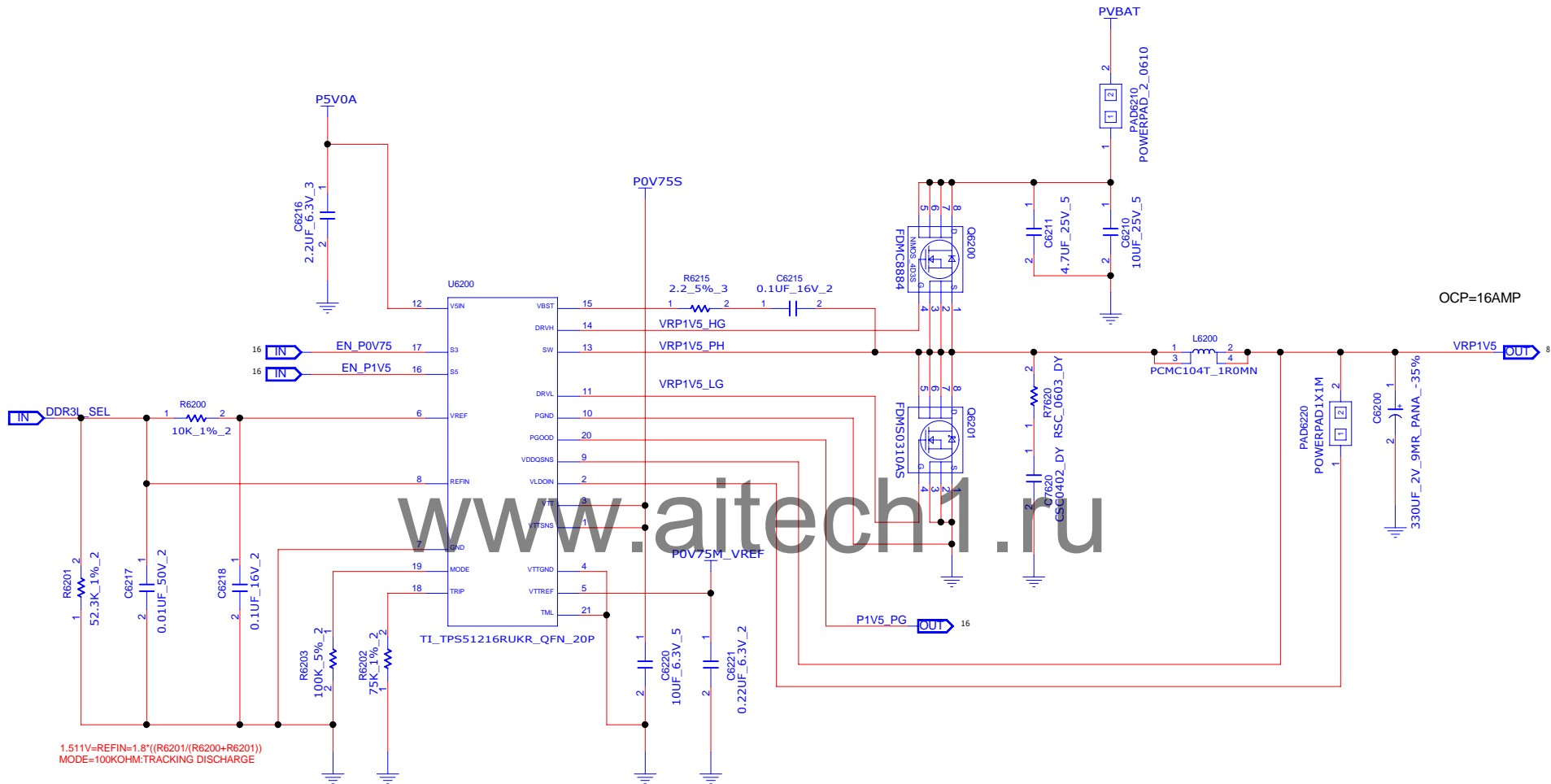
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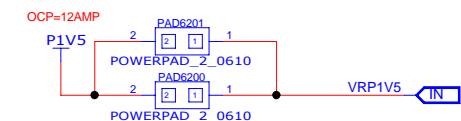




1.511V=REFIN=1.8*/(R6201/(R6200+R6201))
MODE=100KOHM:TRACKING DISCHARGE

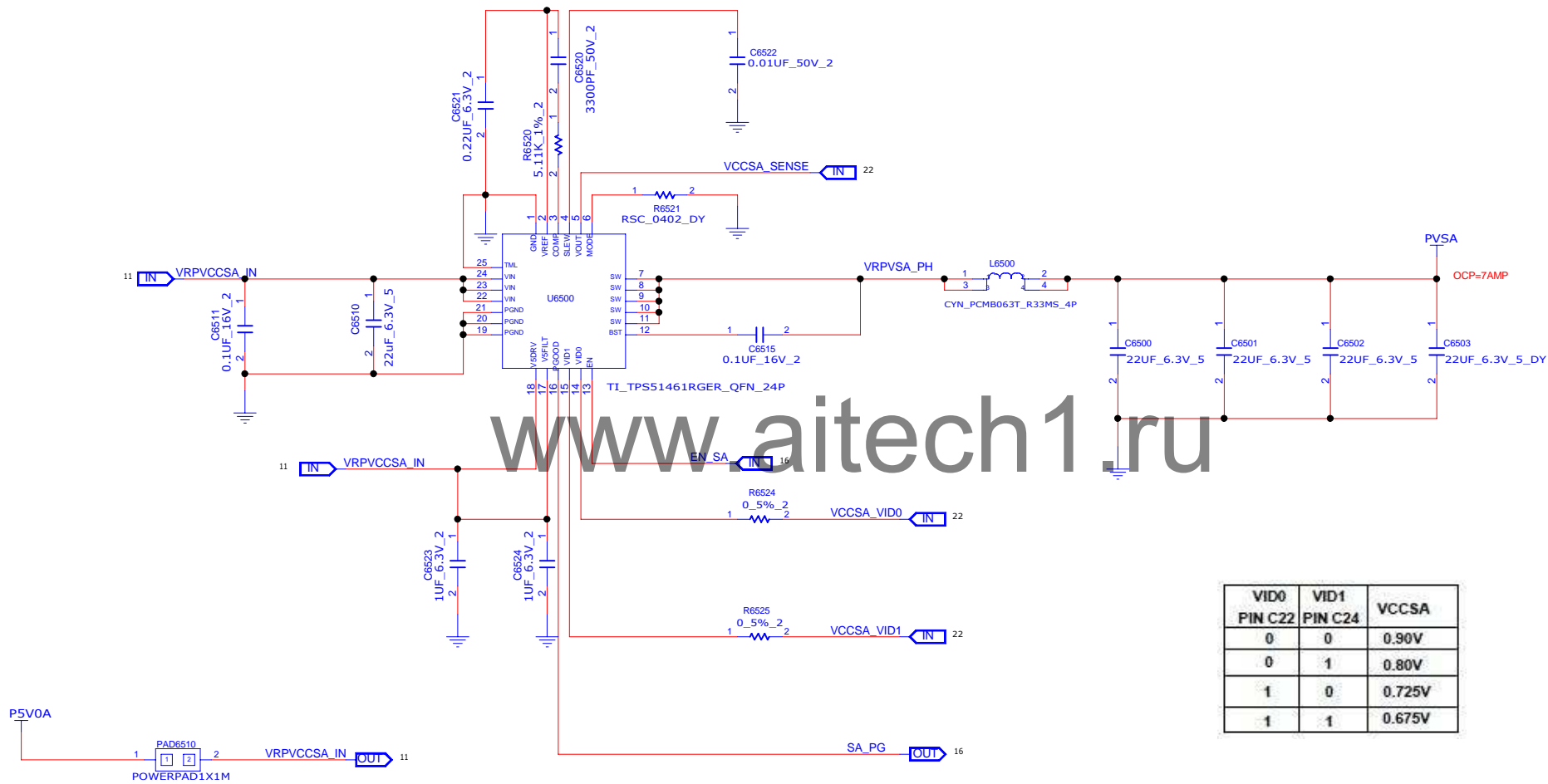
Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)



INVENTEC

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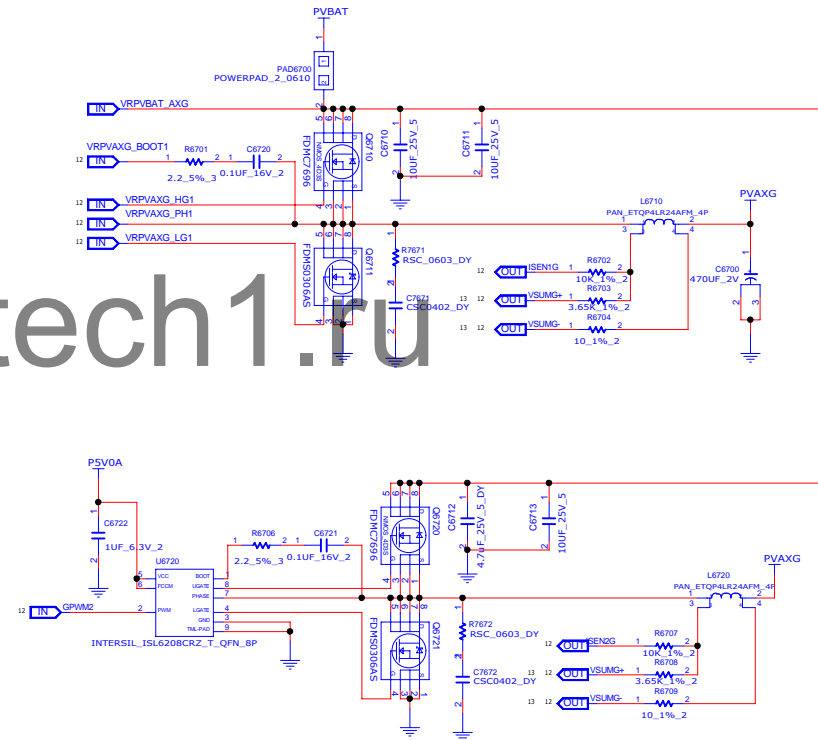
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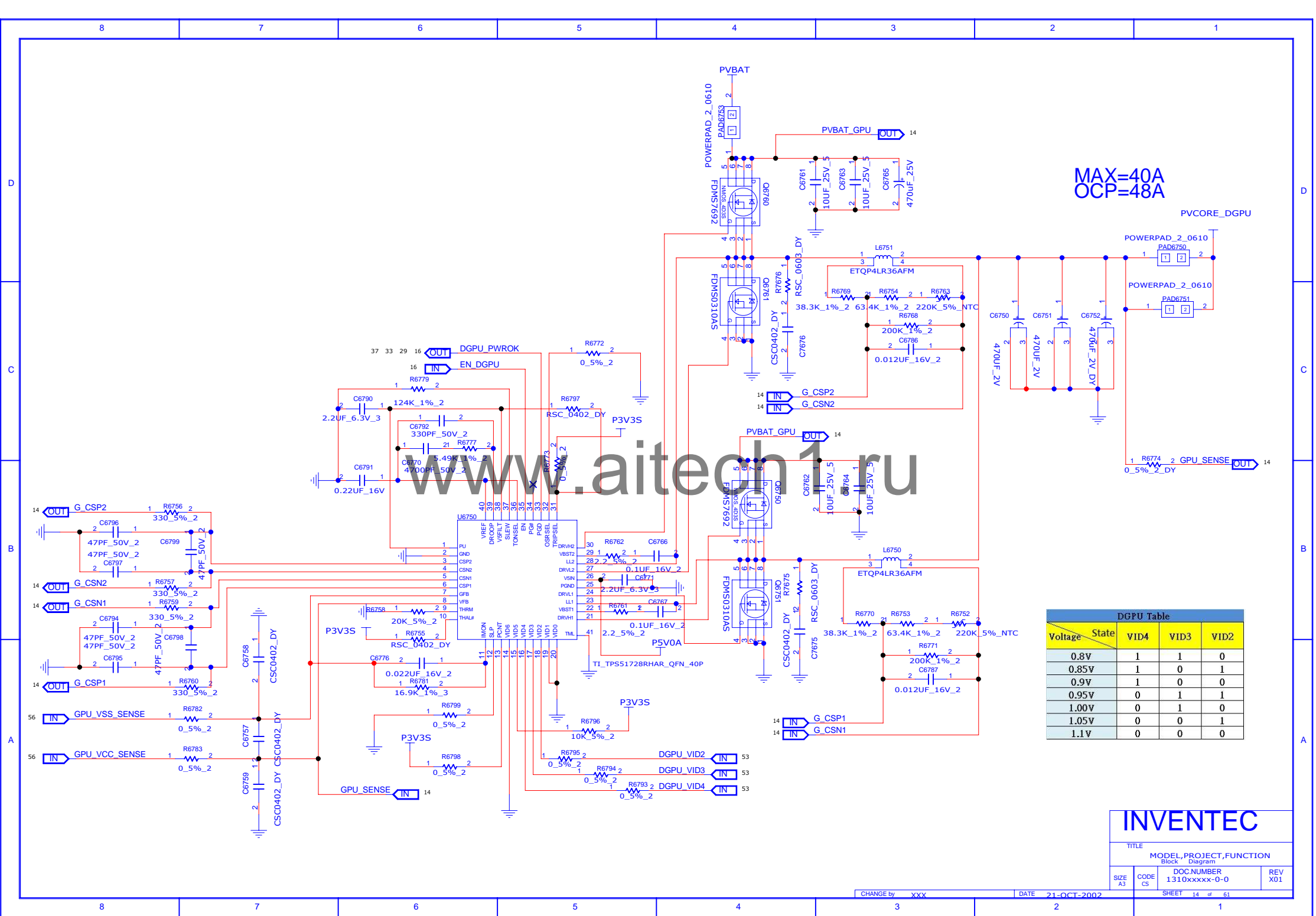
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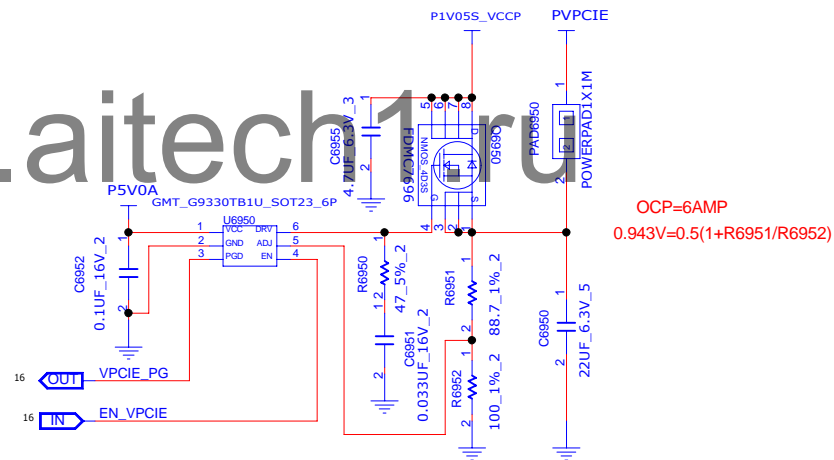
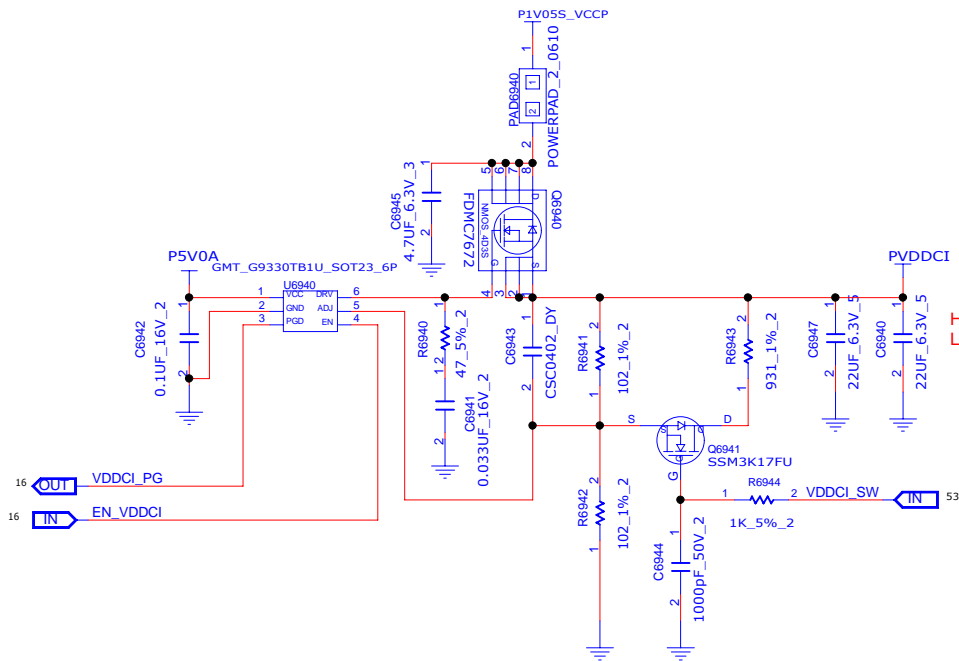
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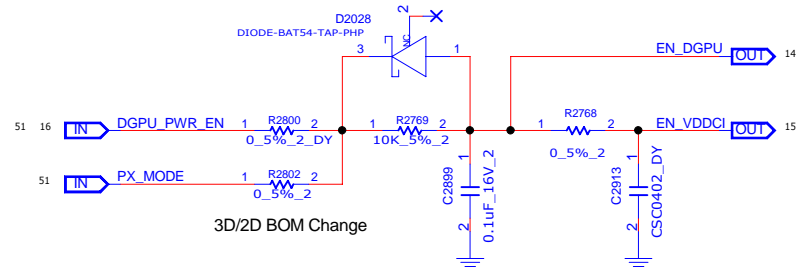
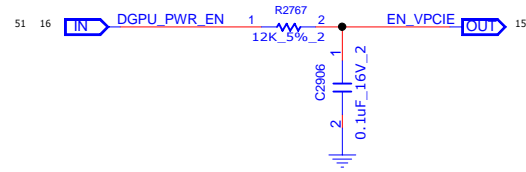
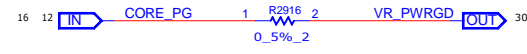
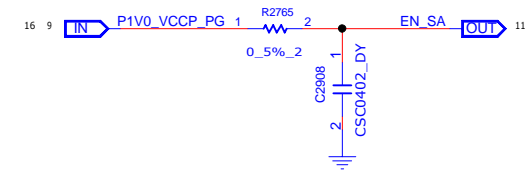
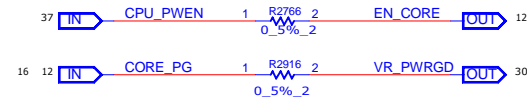
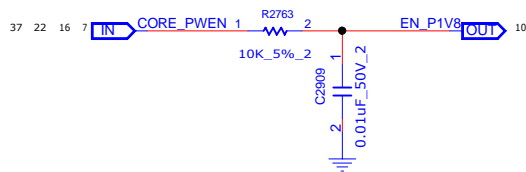
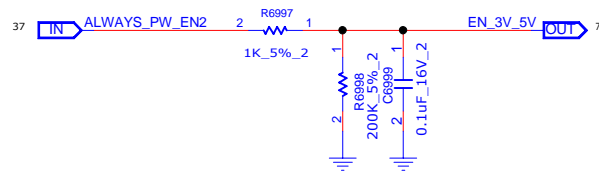
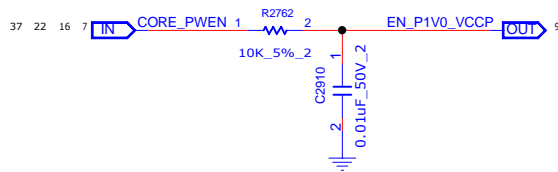
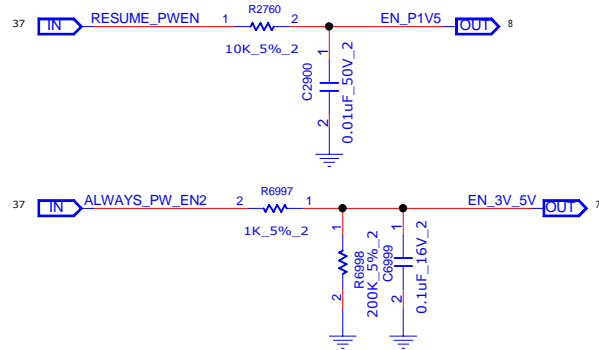
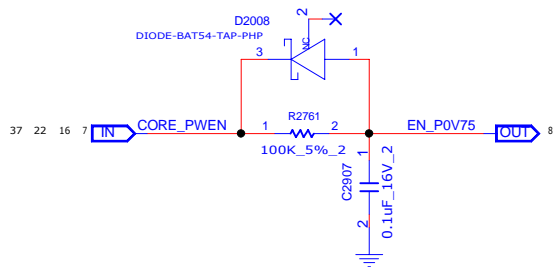






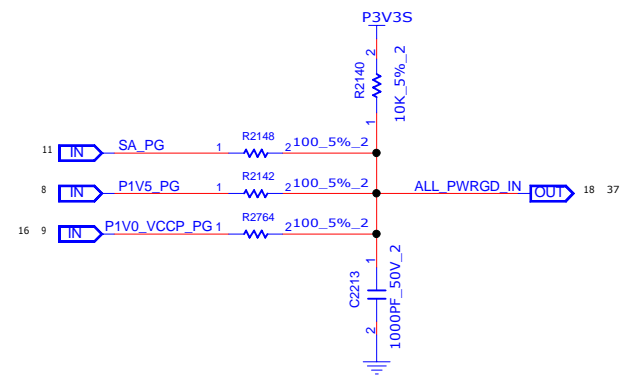
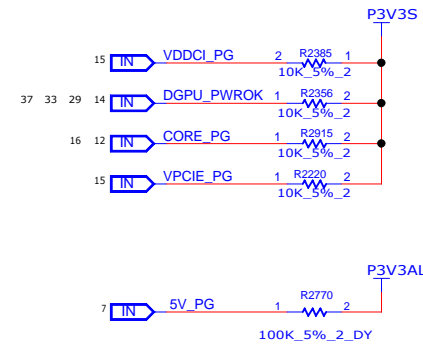
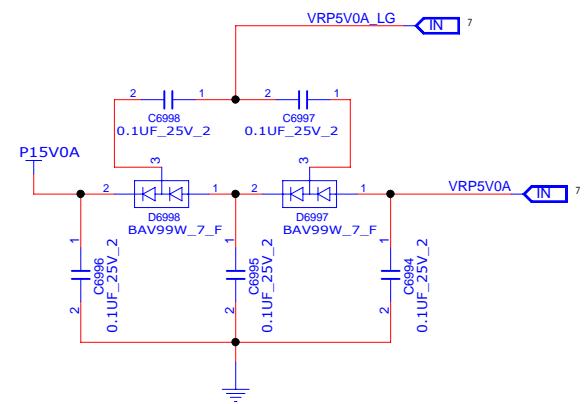
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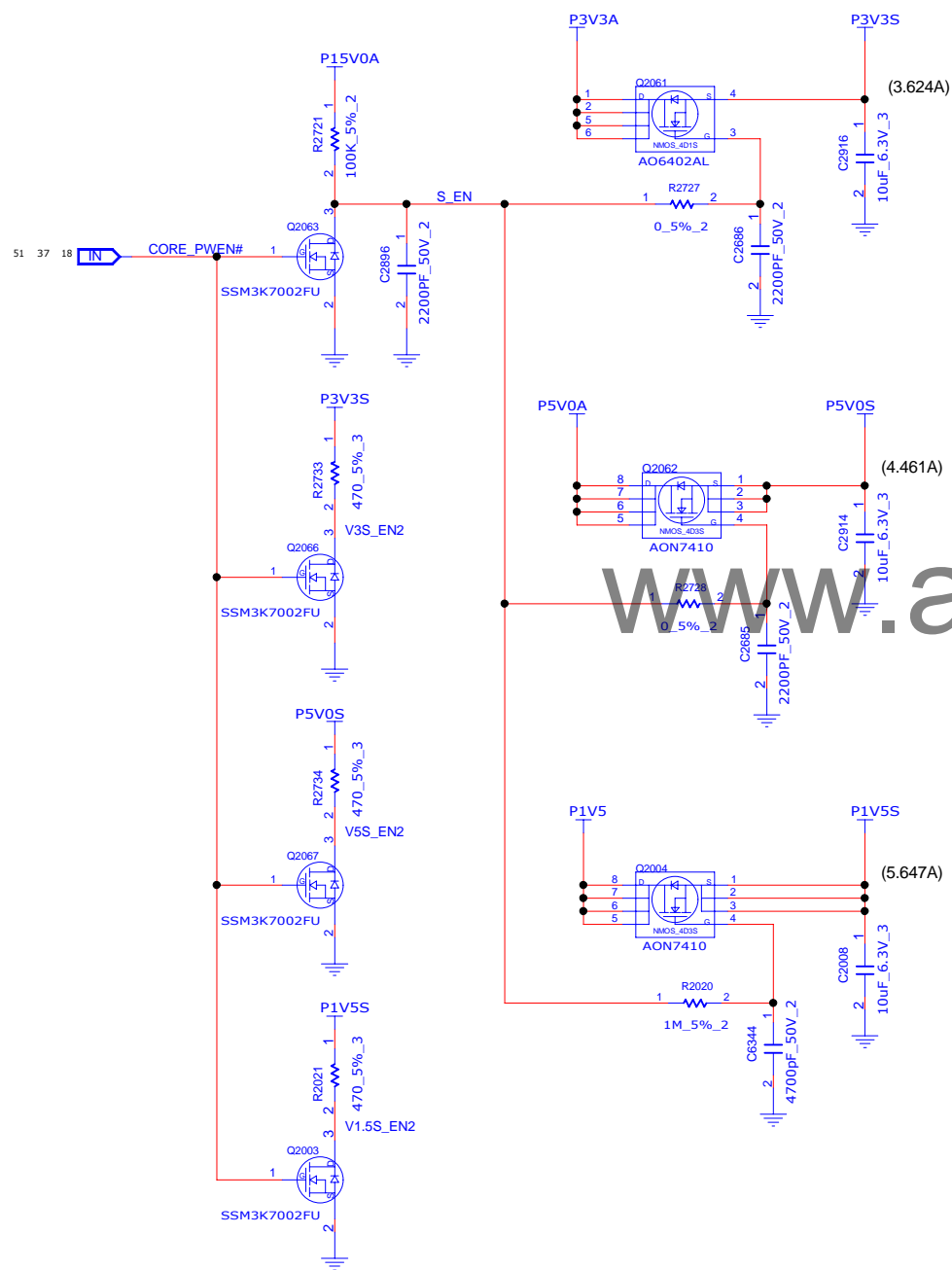


3D/2D BOM Change

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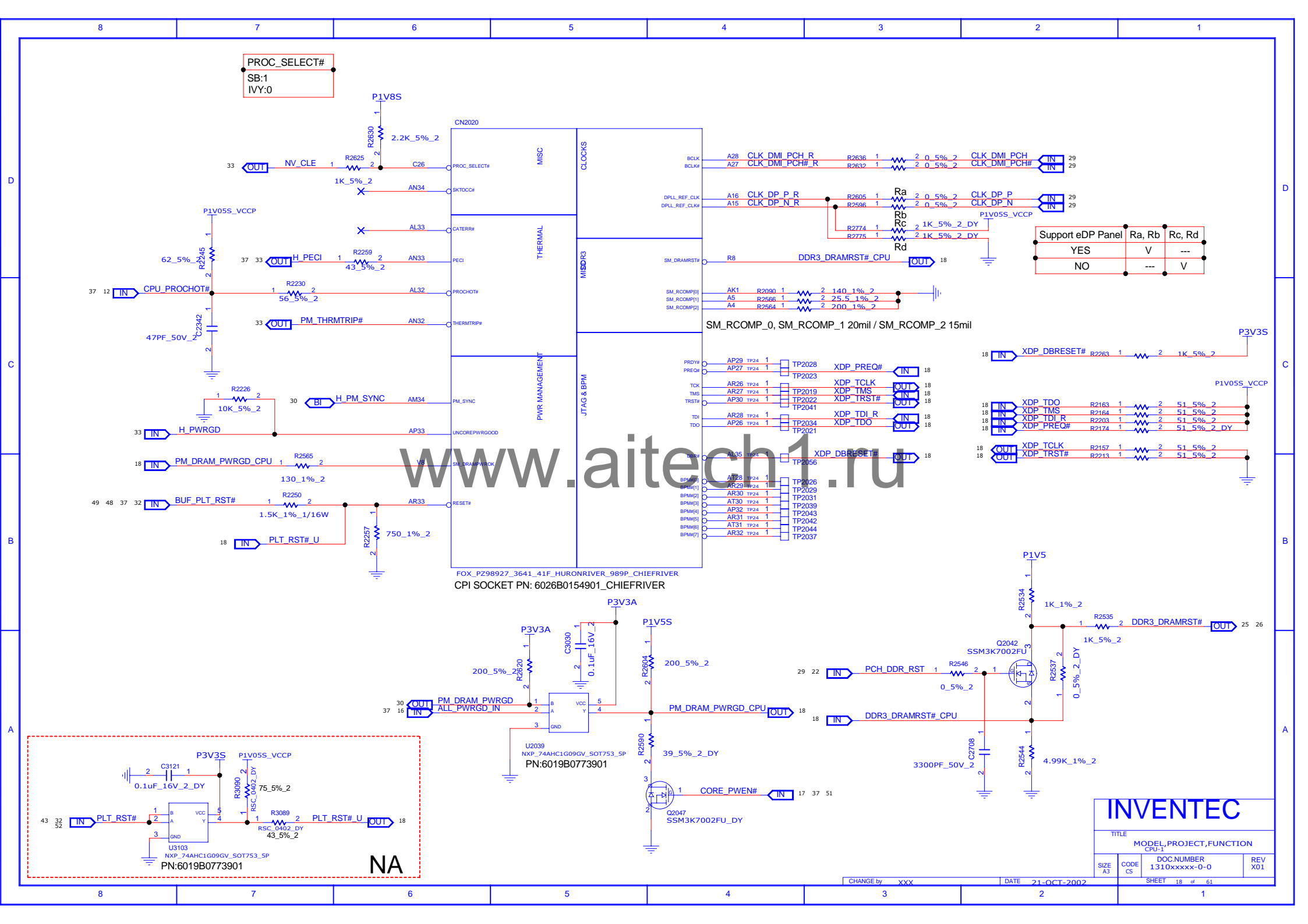
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INVENTEC

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SIZE	CODE	DOC NUMBER	REV
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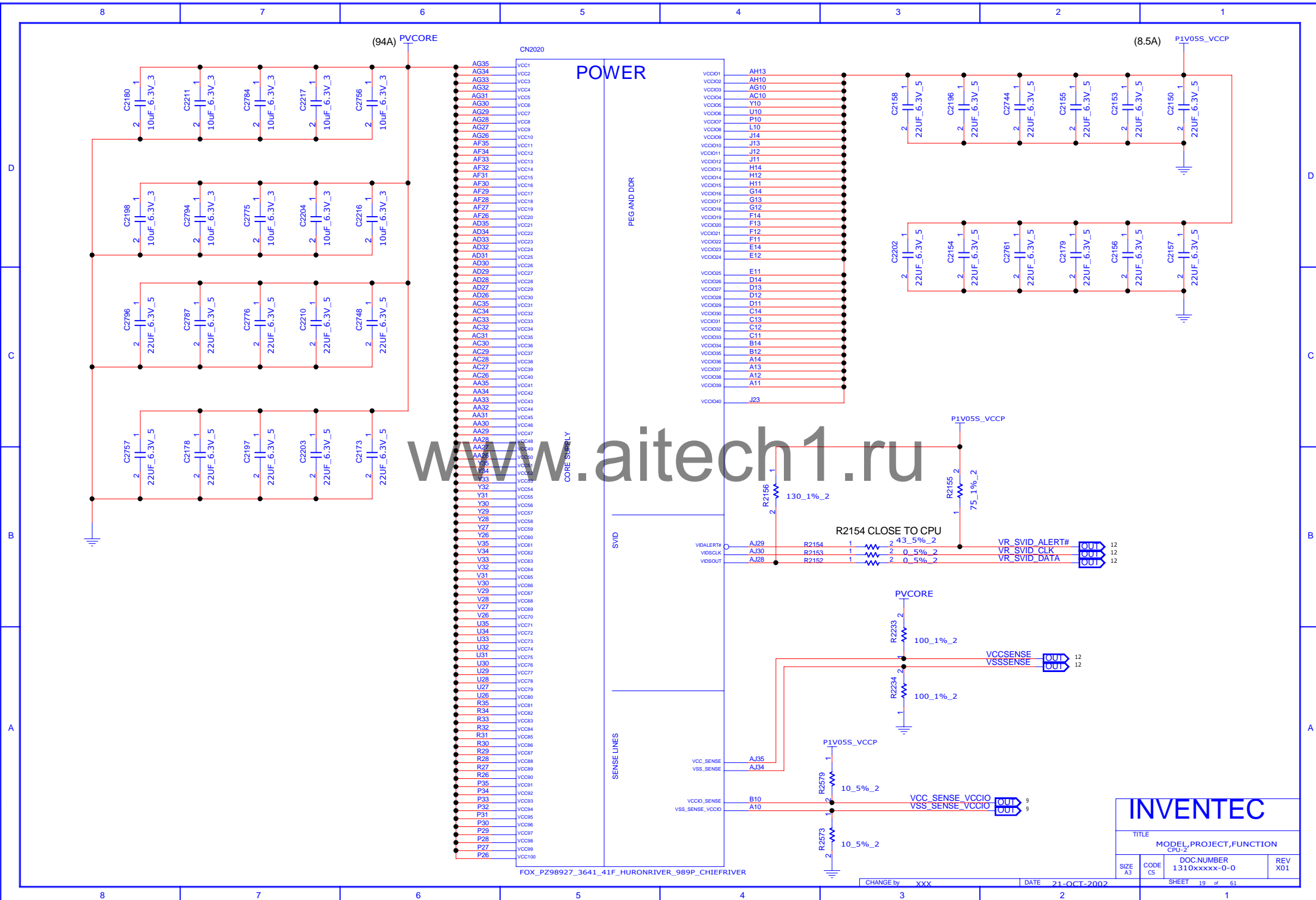


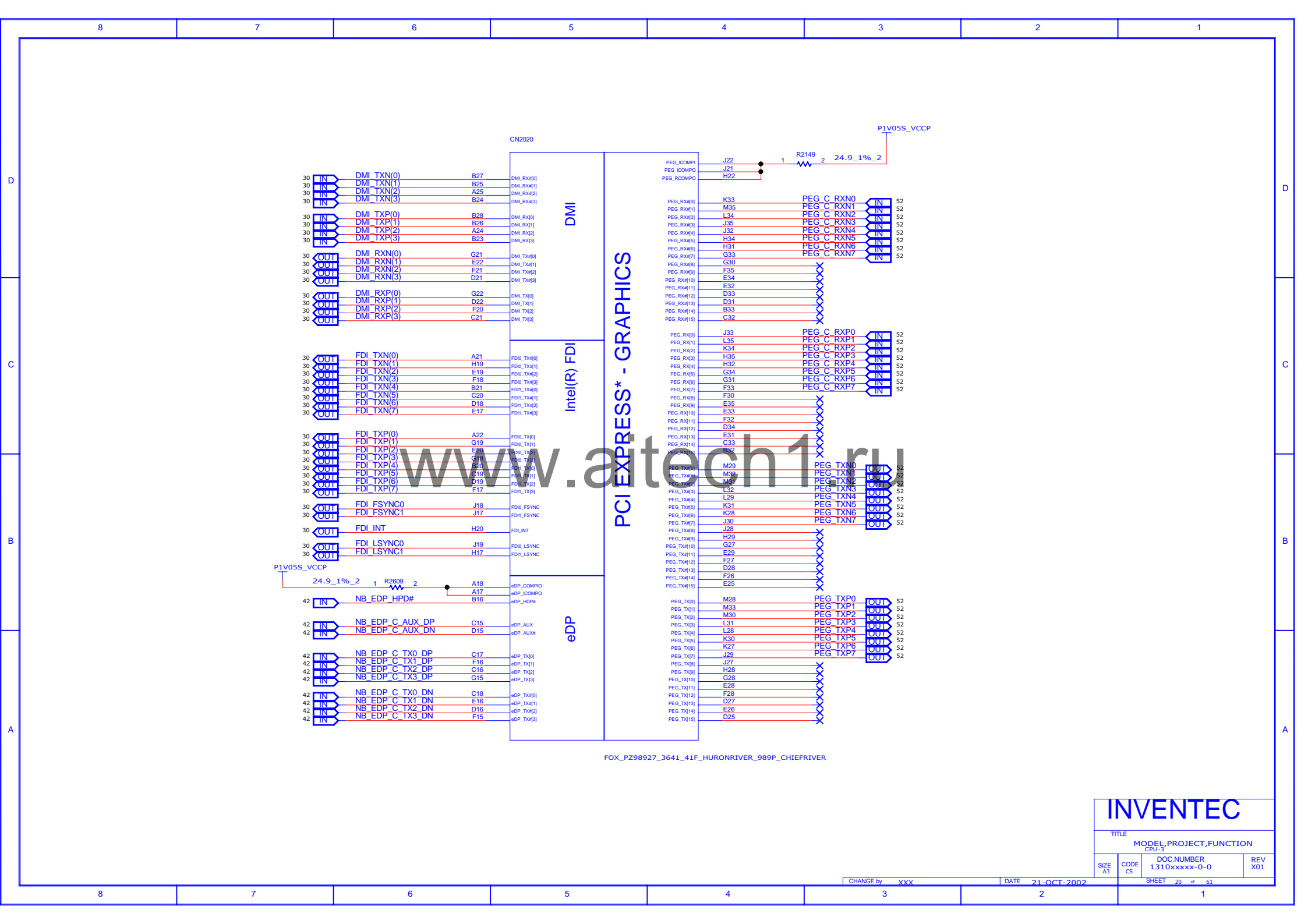
PROC_SELECT#
SB:1
IVY:0

Support eDP Panel	Ra, Rb	Rc, Rd
YES	V	---
NO	---	V

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INVENTEC			
TITLE			
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A3	CS	1310xxxxx-0-0	X01





FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFTRIVER

INVENTEC

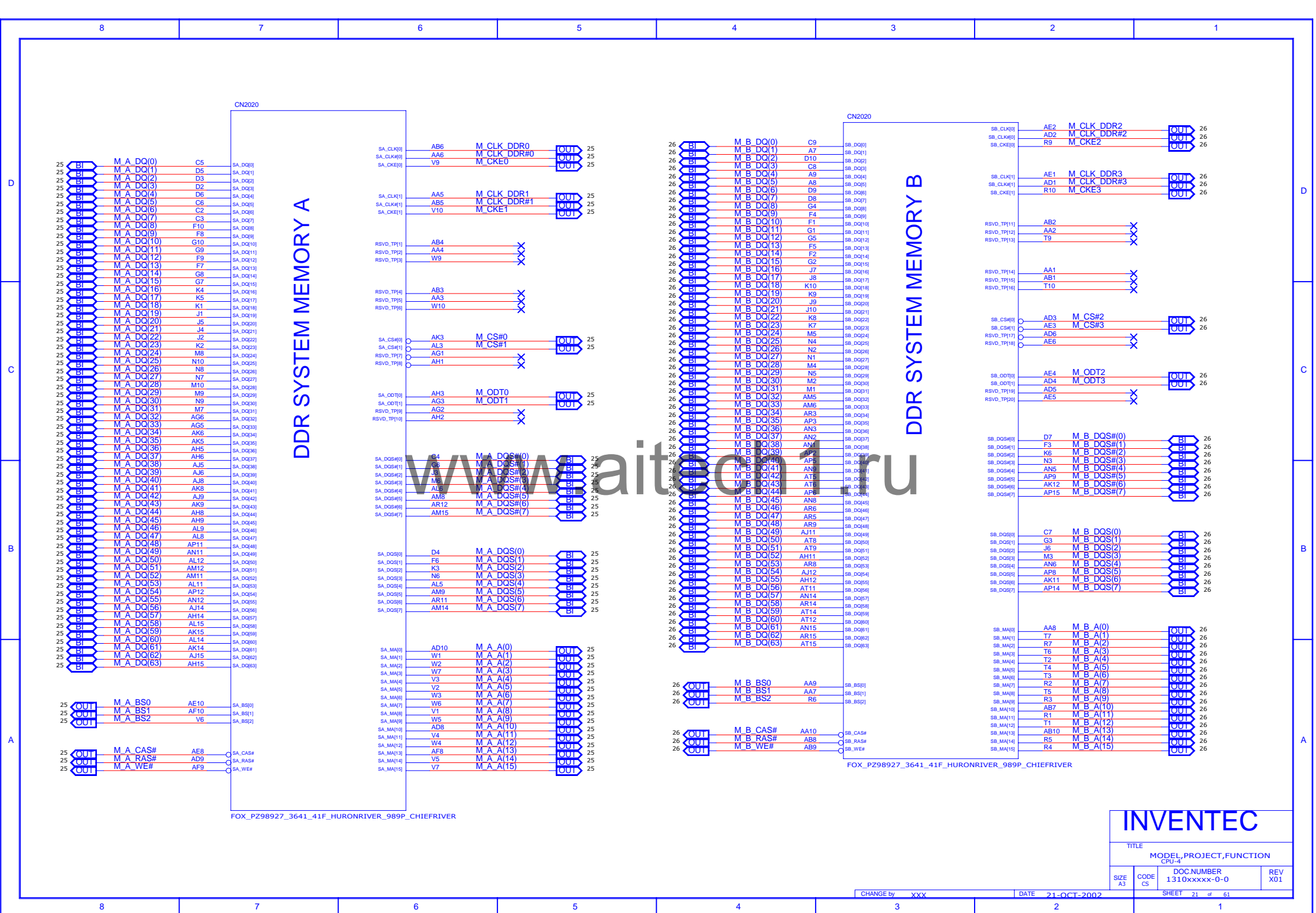
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MODEL, PROJECT, FUNCTION
CPU-3

DOC NUMBER
1310xxxxx-0-0

REV
X01

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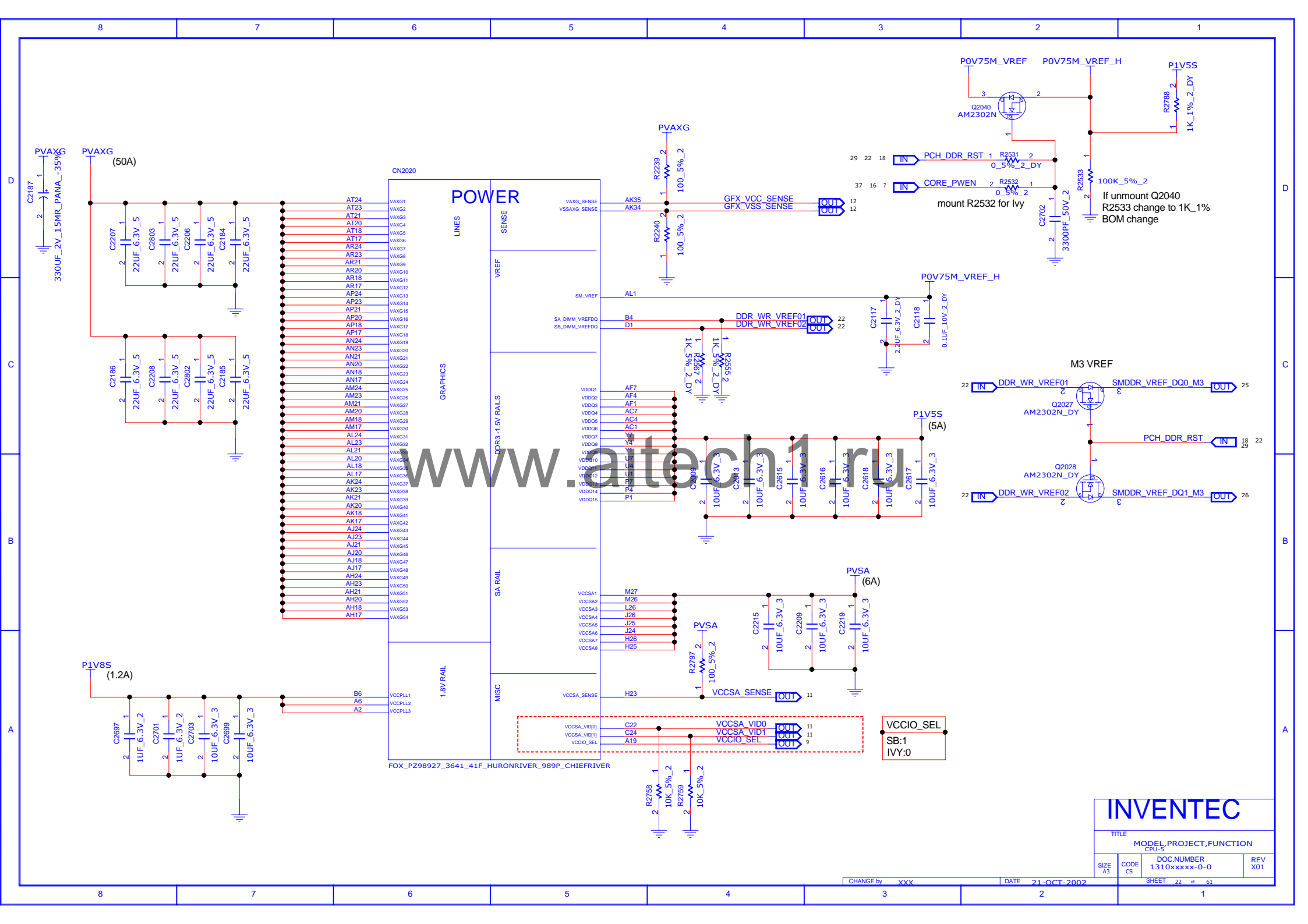


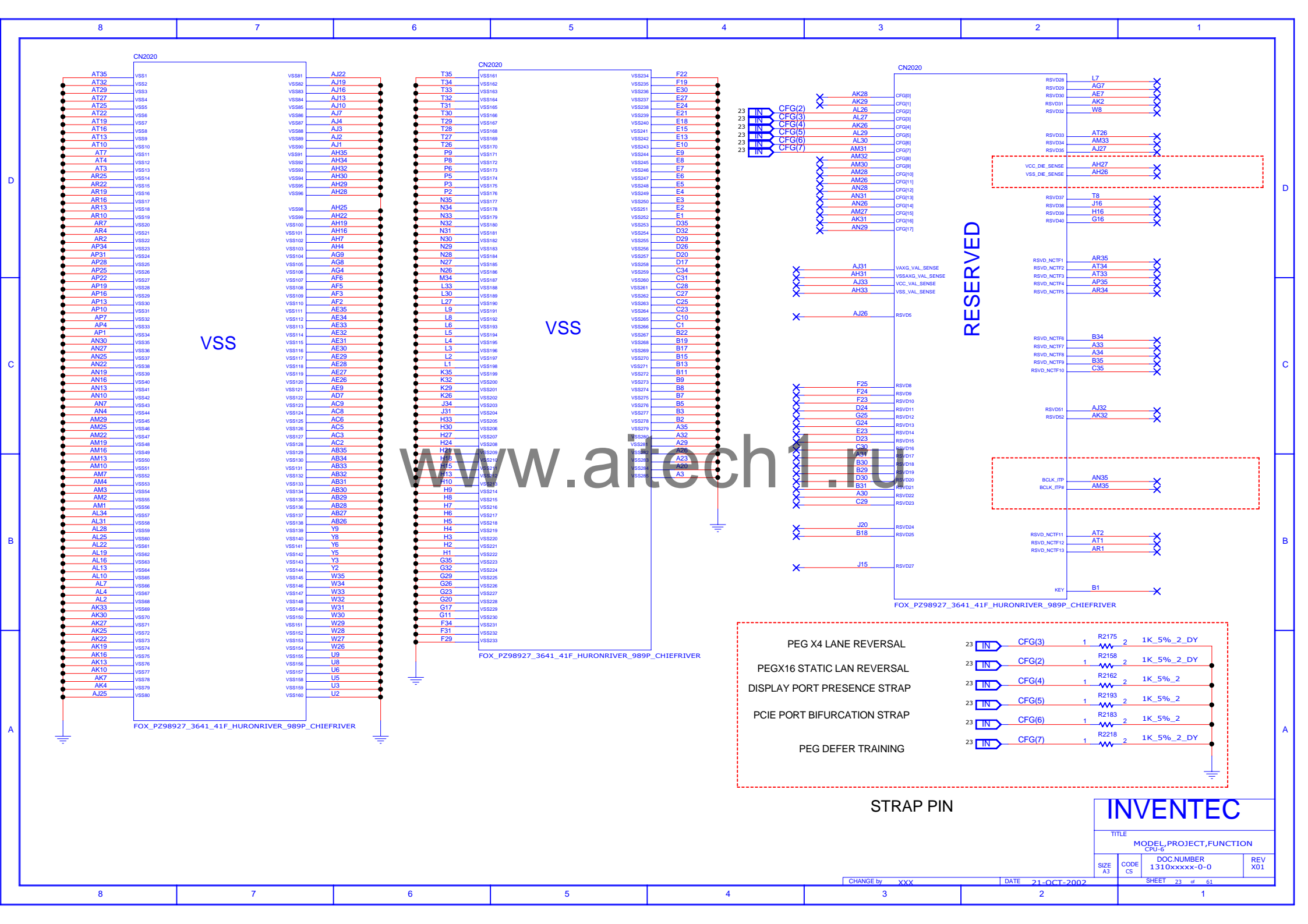
INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
CPU-4

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

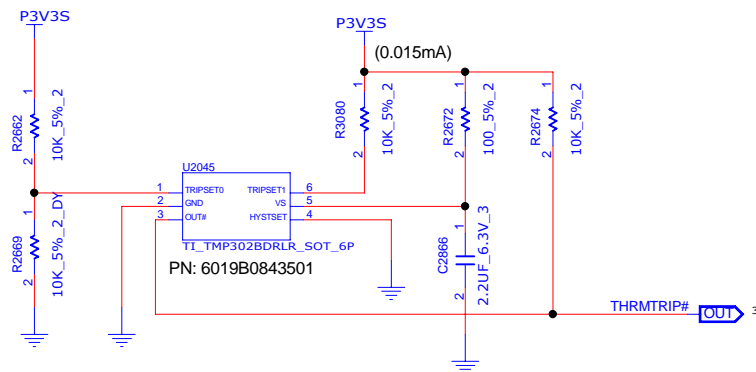
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FAN CONN

TRIP _{SET1}	TRIP _{SET0}	TMP302B
GND	GND	+70°C
GND	V _S	+75°C
V _S	GND	+80°C
V _S	V _S	+85°C

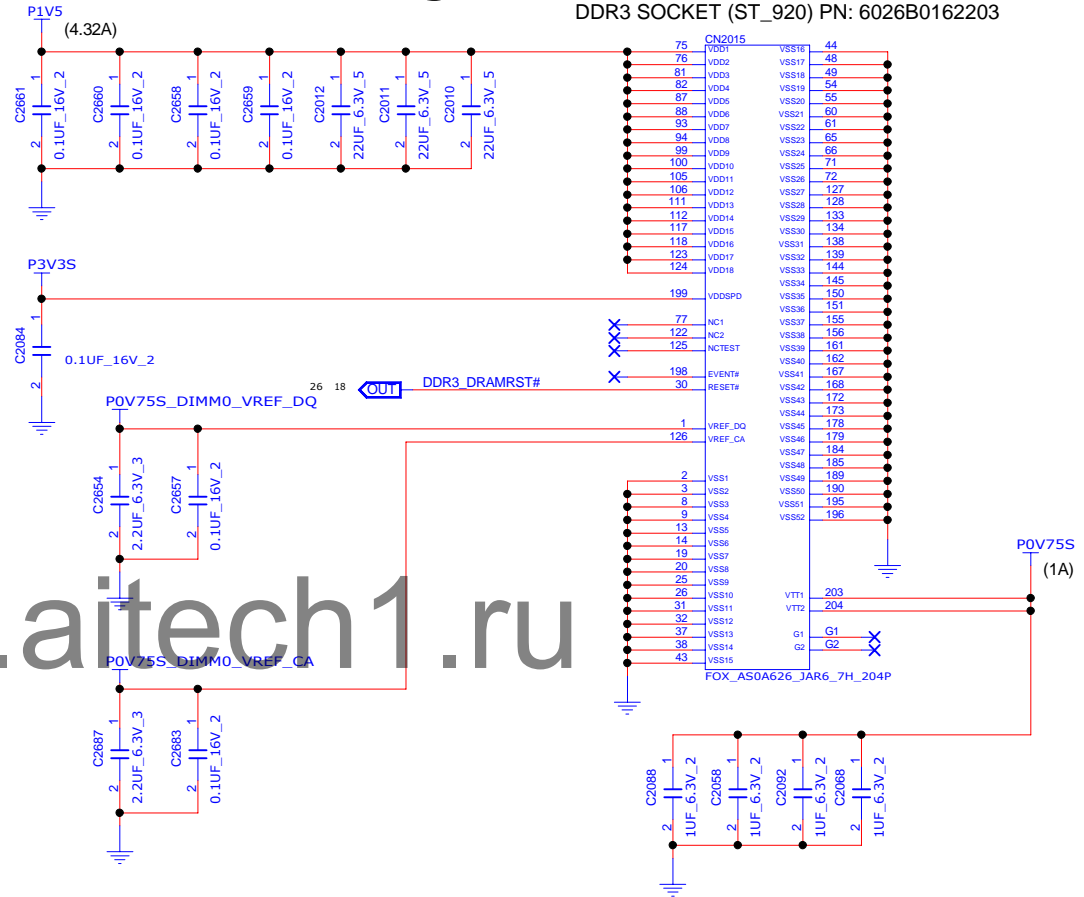
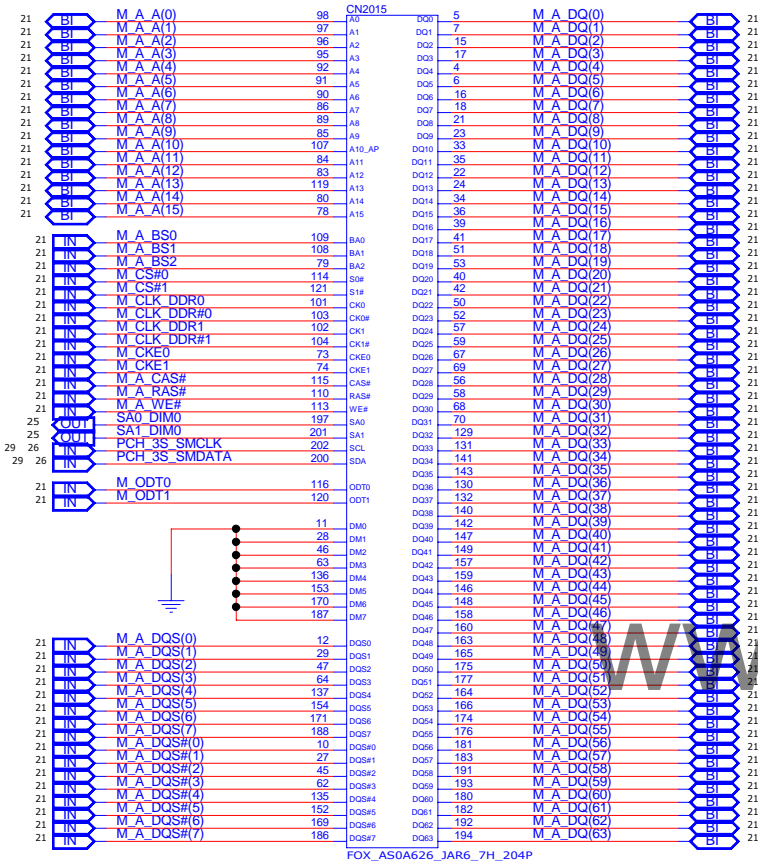


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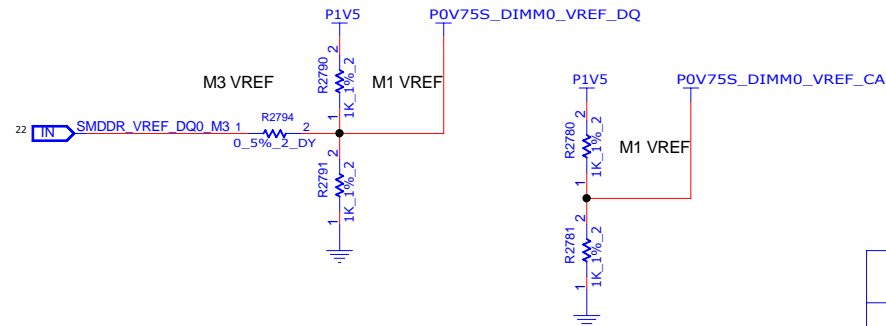
RVS

DDR3 SO-DIMM 0

DDR3 SOCKET (ST_920) PN: 6026B0162203



NOTE:
IF SA0_DIM0=0, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30
IF SA0_DIM0=1, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
DDR3-1

SIZE	CODE	DOC. NUMBER	REV
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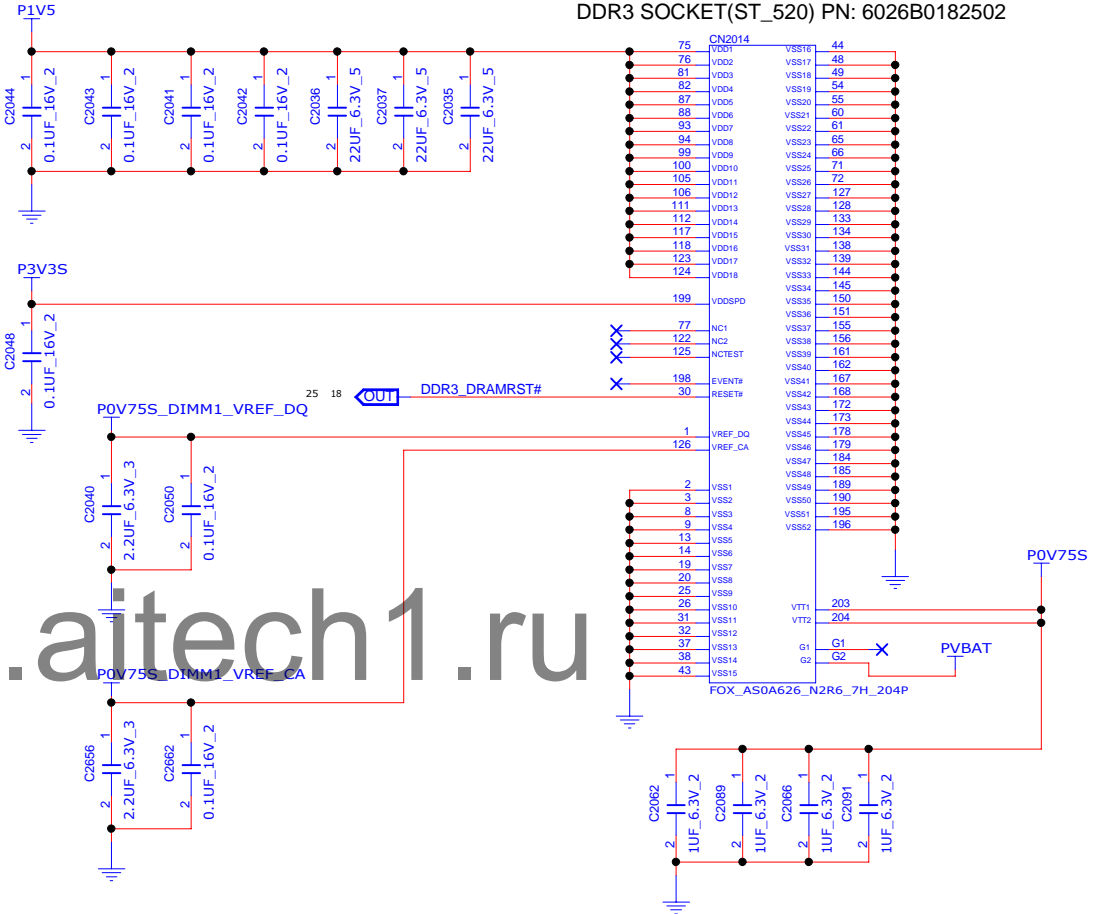
CHANGE by XXX

DATE 21-OCT-2002

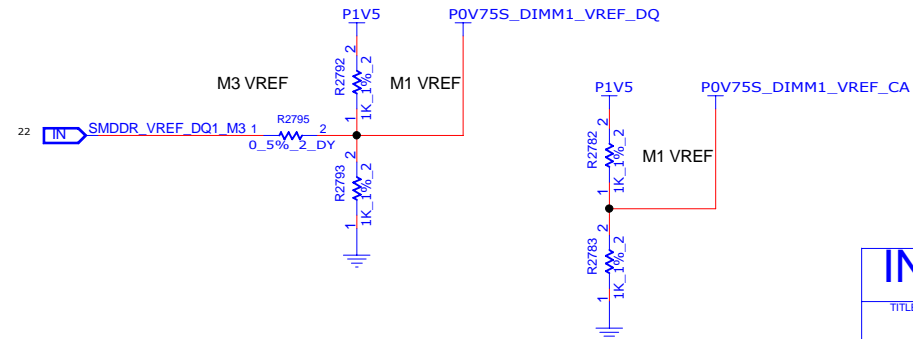
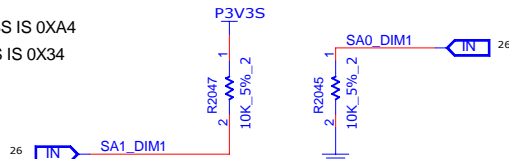
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RVS DDR3 SO-DIMM 1

DDR3 SOCKET(ST_520) PN: 6026B0182502



NOTE:
SO-DIMMB SPD ADDRESS IS 0XA4
SO-DIMMB TS ADDRESS IS 0X34



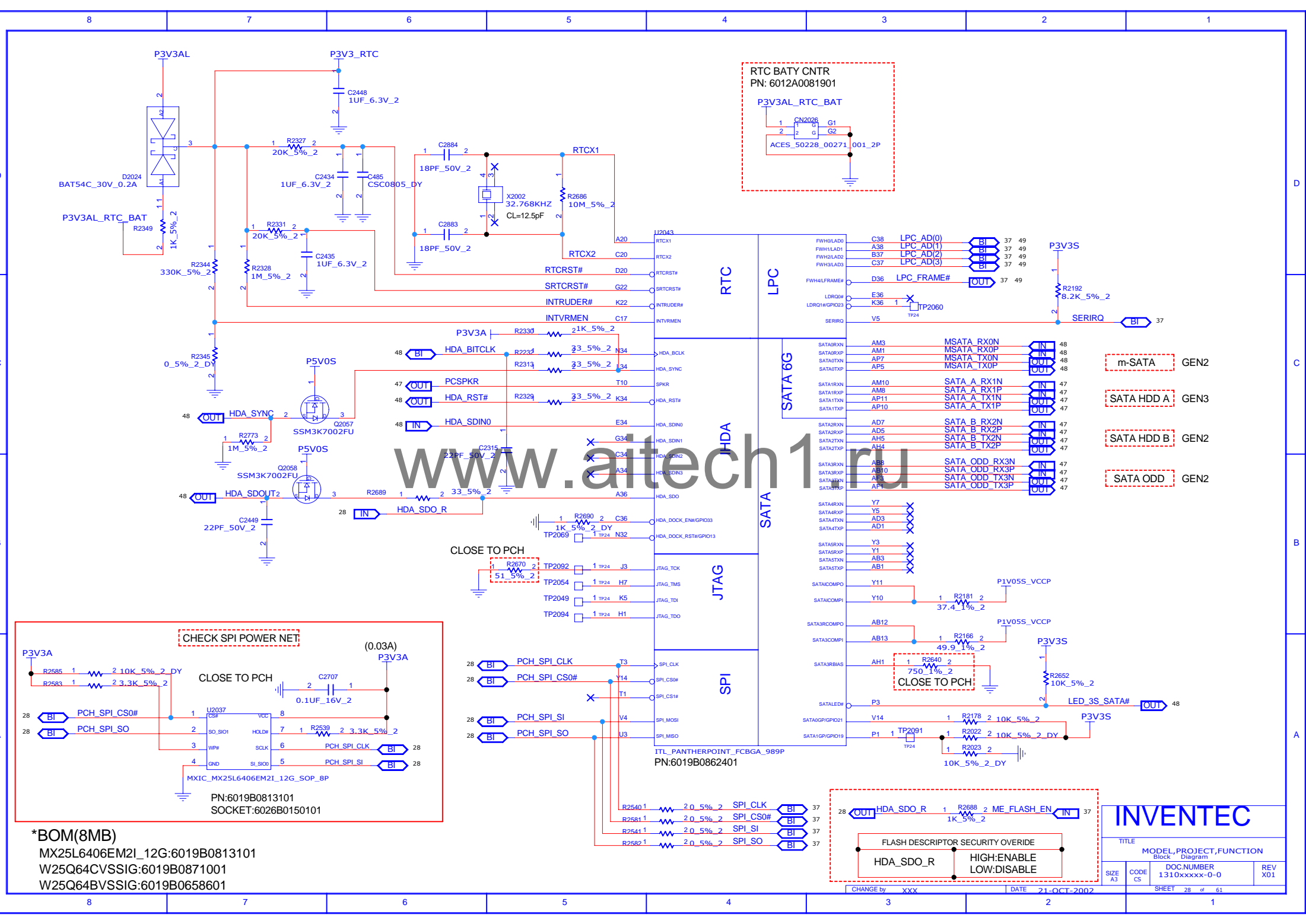
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TITLE
MODEL PROJECT FUNCTION
DDR3*2

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

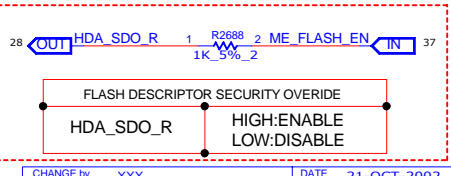
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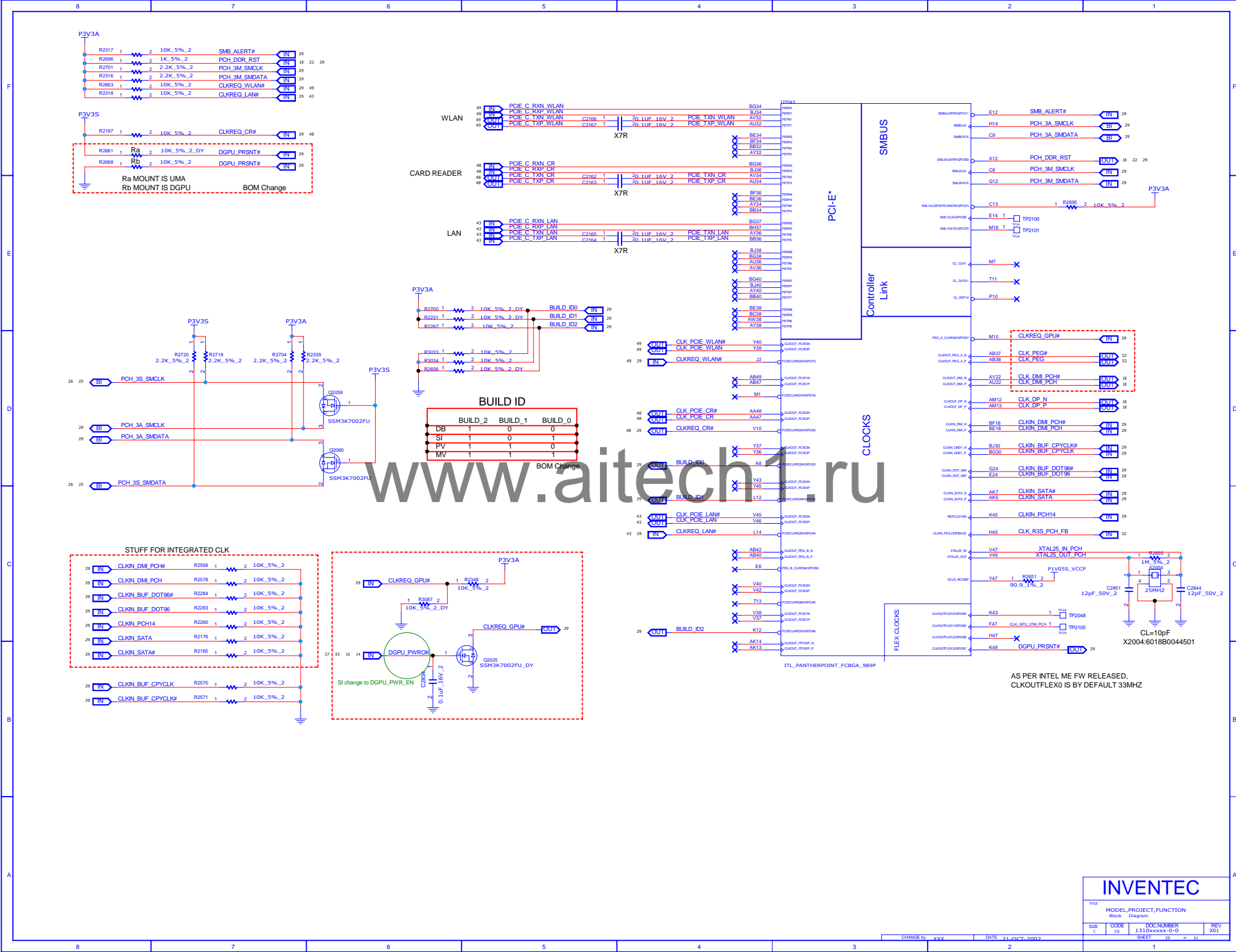


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W25Q64BVSSIG:6019B0658601

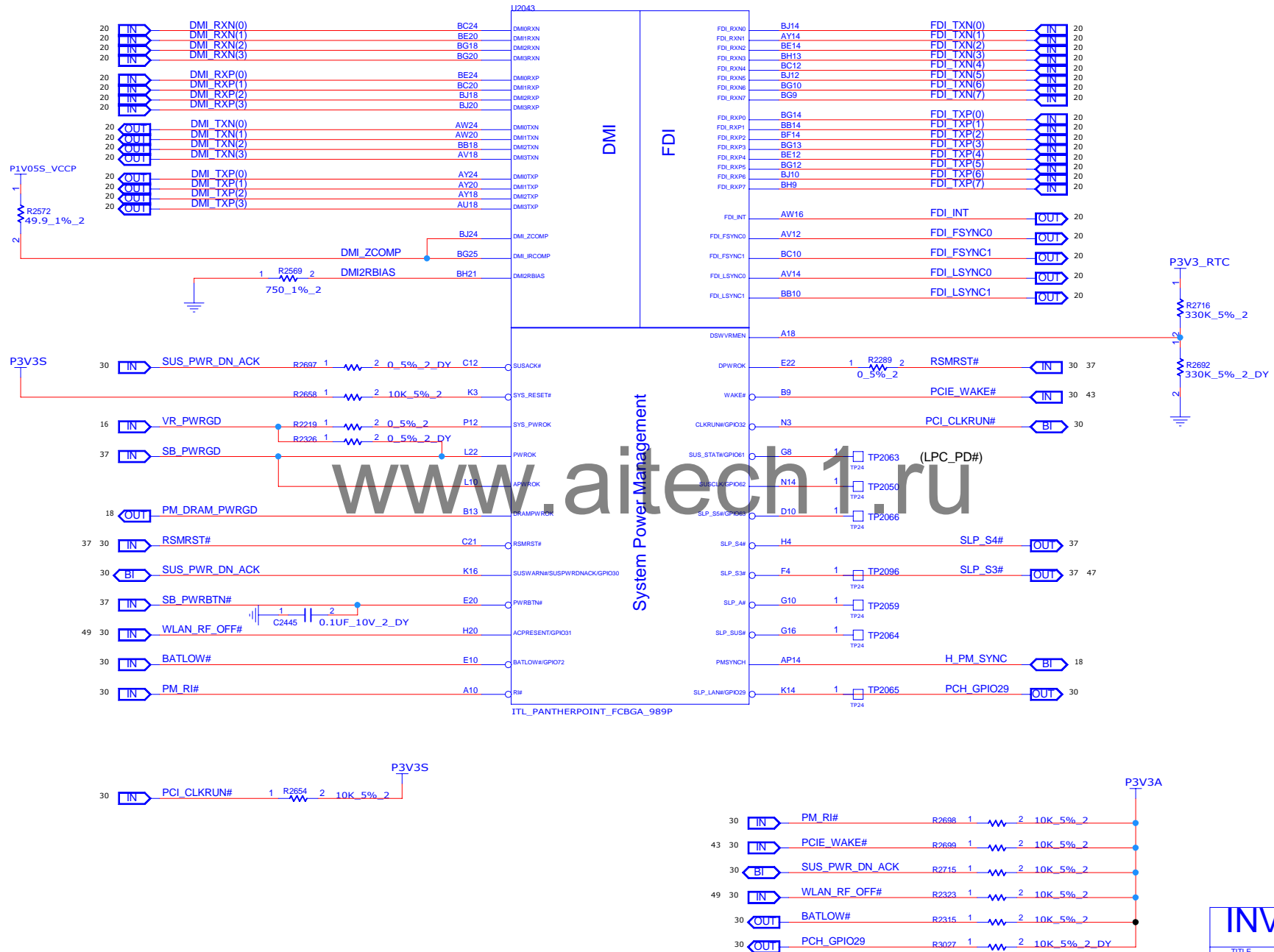
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NOTE:1.SLP_SUS AND SUSACK# ARE NC IF DSW IS NOT SUPPORTED
2.DPWROK SHOULD CONNECT TO RSMRST# IF DSW NOT SUPPORTED

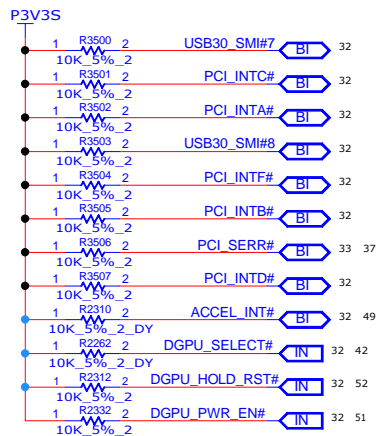


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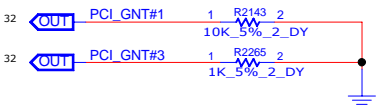
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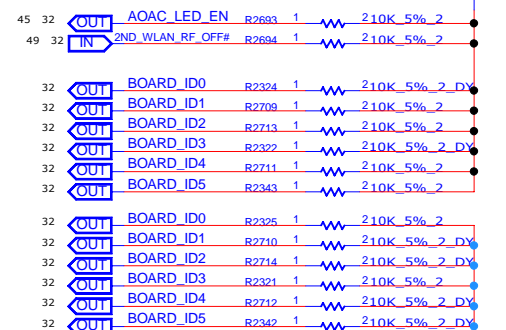
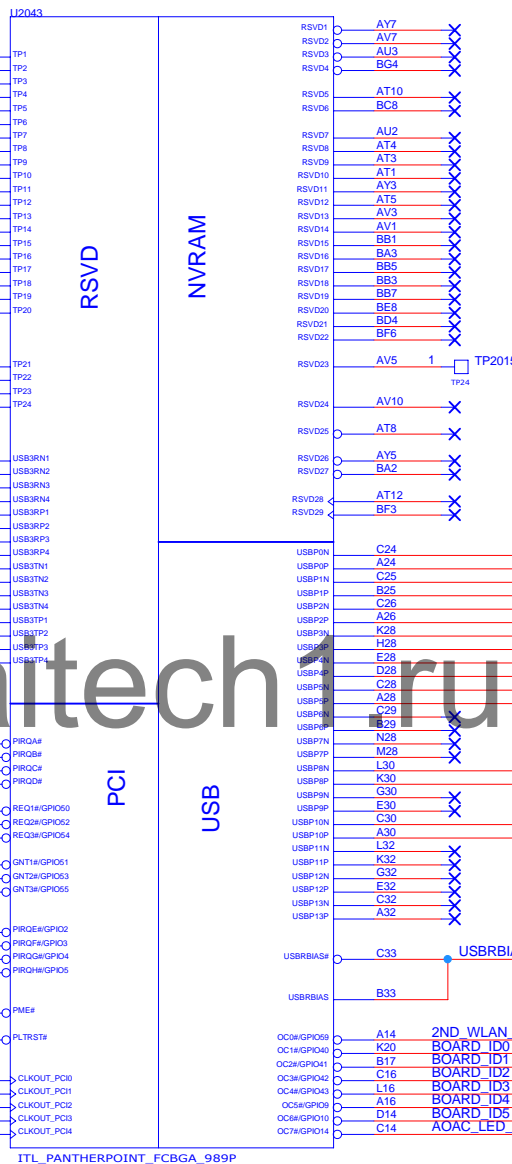
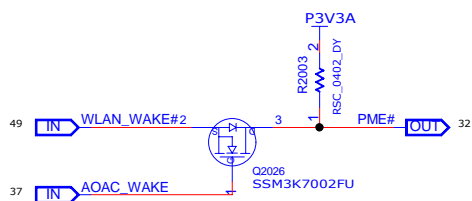
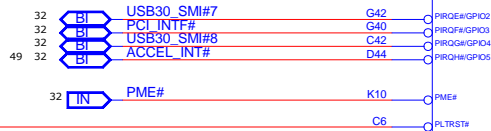
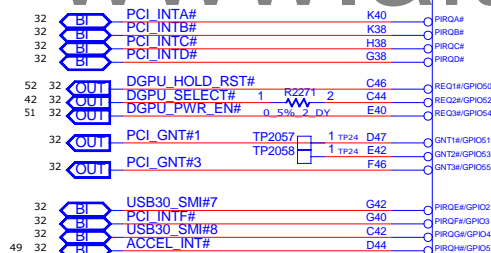
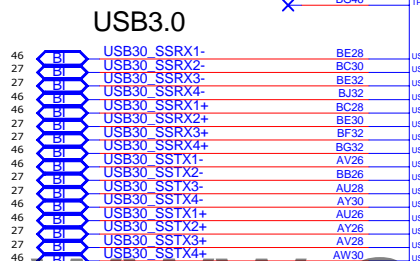
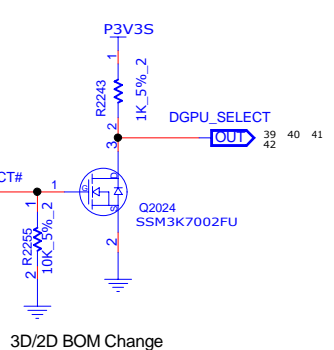
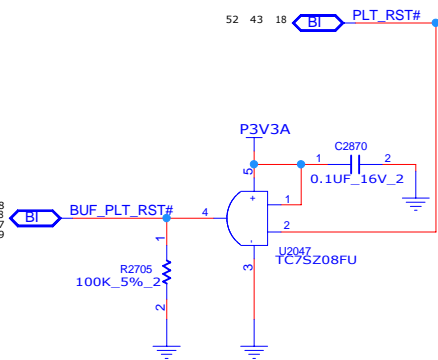
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BBSTRAP1	BBSTRAP0	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	PCI
1	1	SPI



PCI_GNT#3
LOW- A16 SWAP OVERRIDE
/ TOP-BLOCK SWAP OVERRIDE ENABLED



BOARD ID	ID0	ID1	ID2	ID3	ID4	ID5
DIS(3D)	0	1	1	0	1	1
DIS(2D)	1	0	1	0	1	1
UMA	0	0	1	0	1	1

DEFAULT: DIS(3D)

BOM Change

USB CONN02

USB CONN
on DB

USB CONN01

WIRELESS AUDIO

WEBCAM

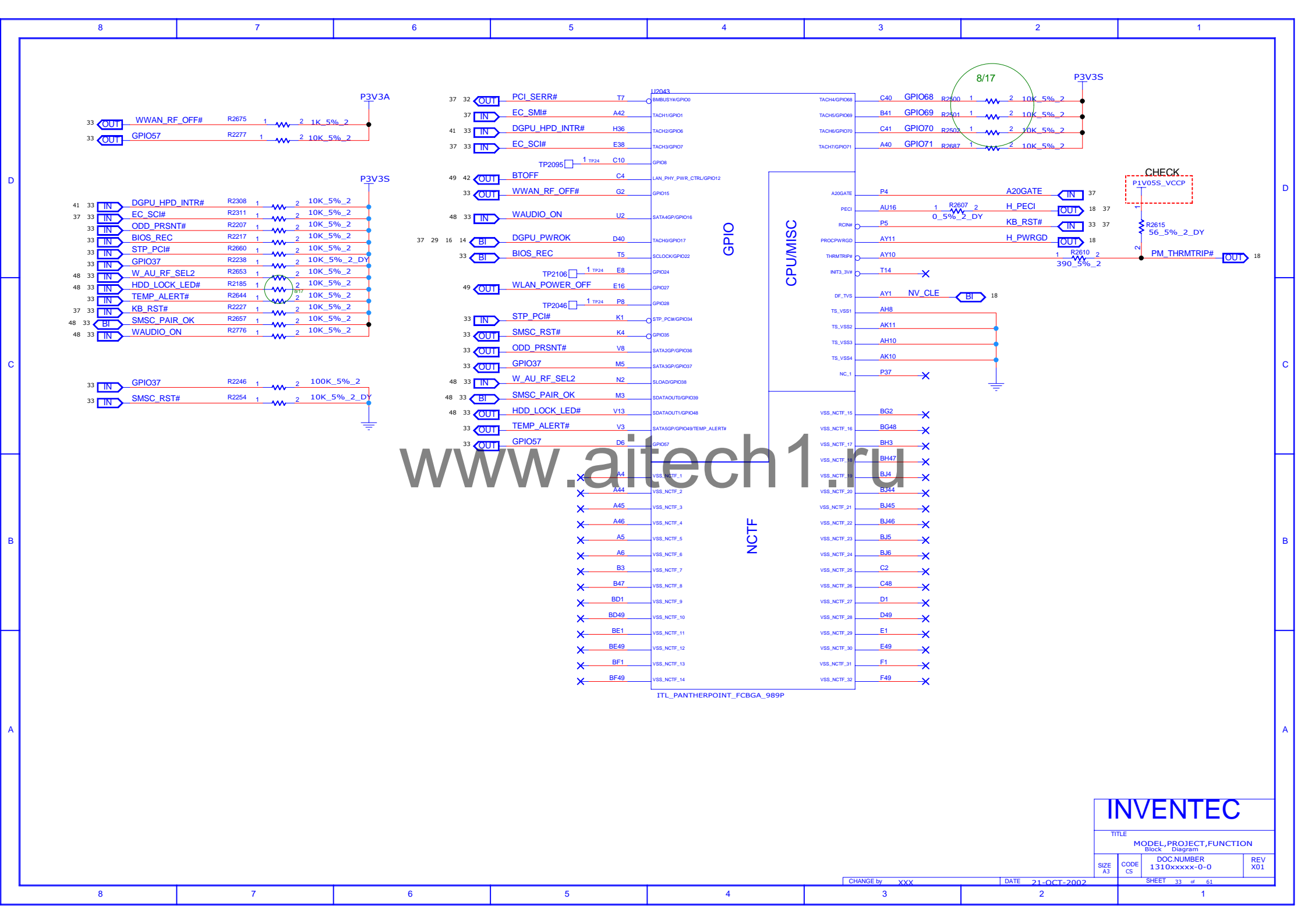
WLAN+BT

BLUETOOTH

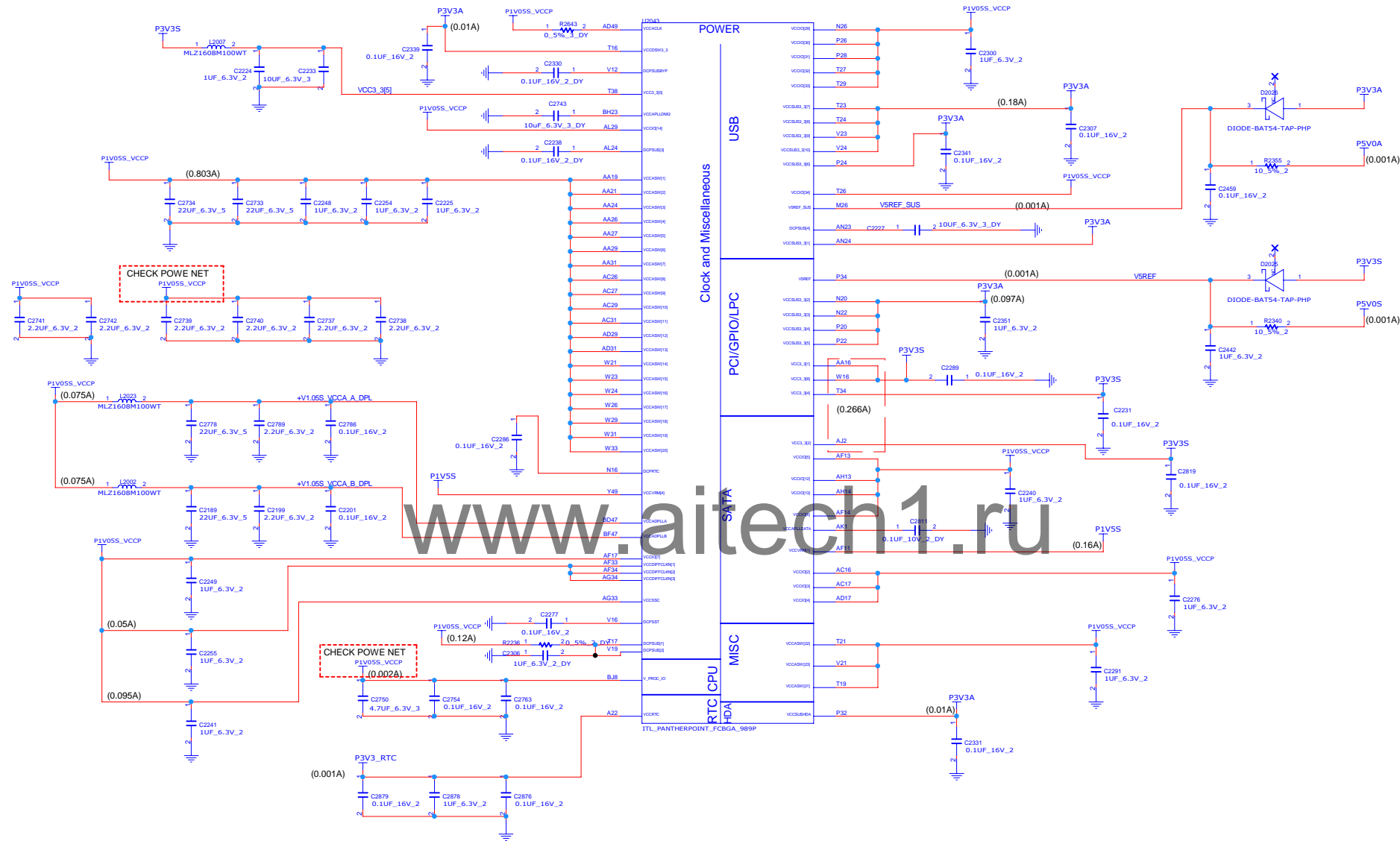
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MODEL,PROJECT,FUNCTION Block Diagram			
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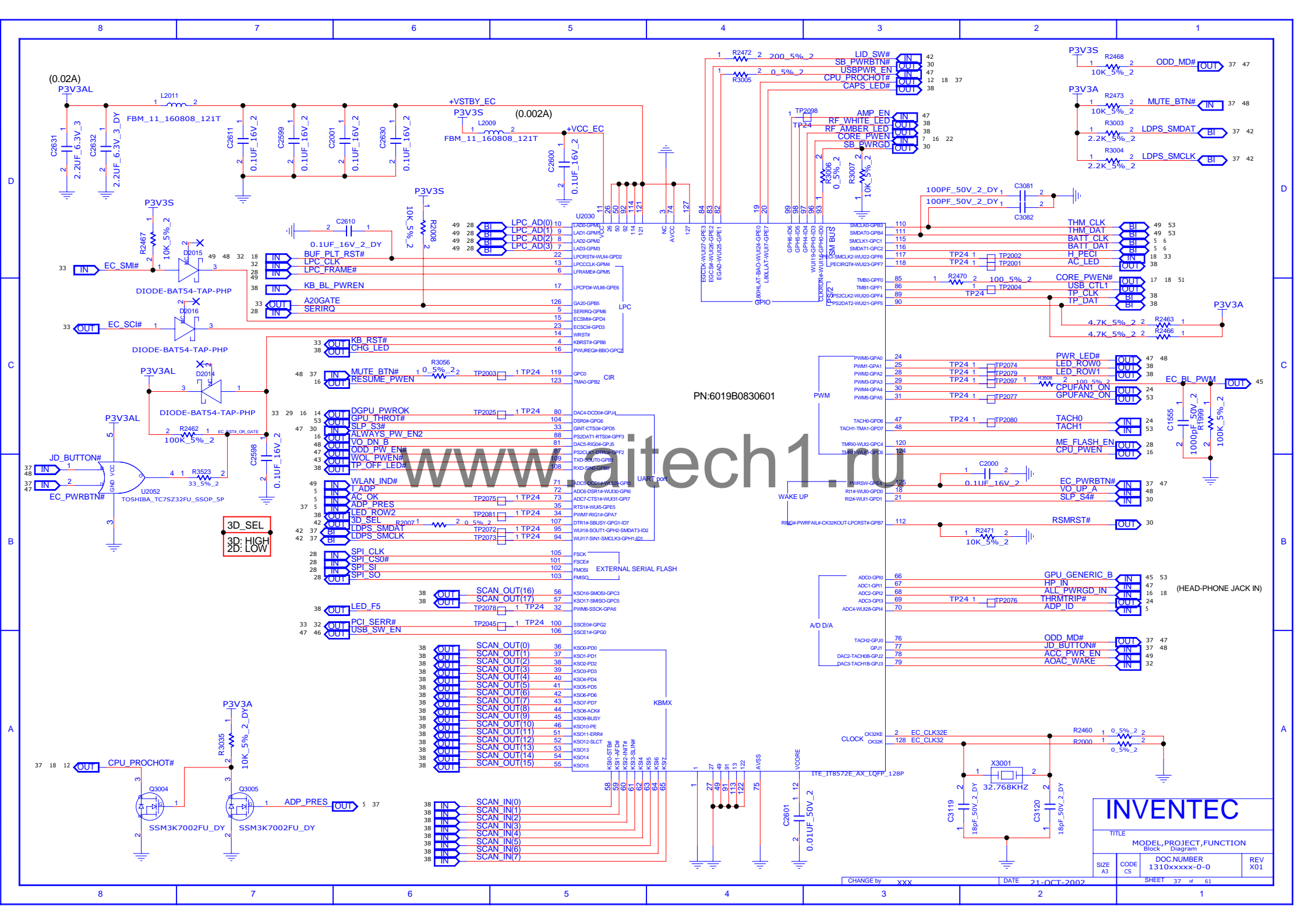
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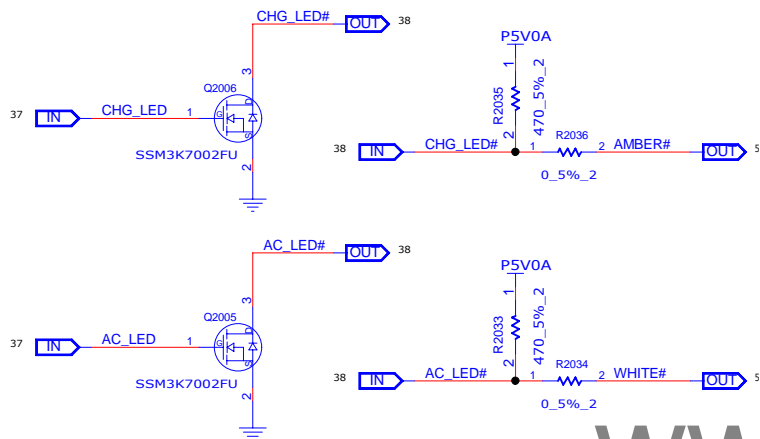
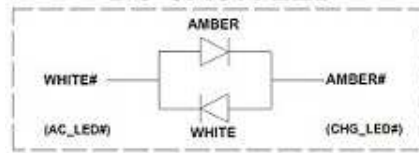
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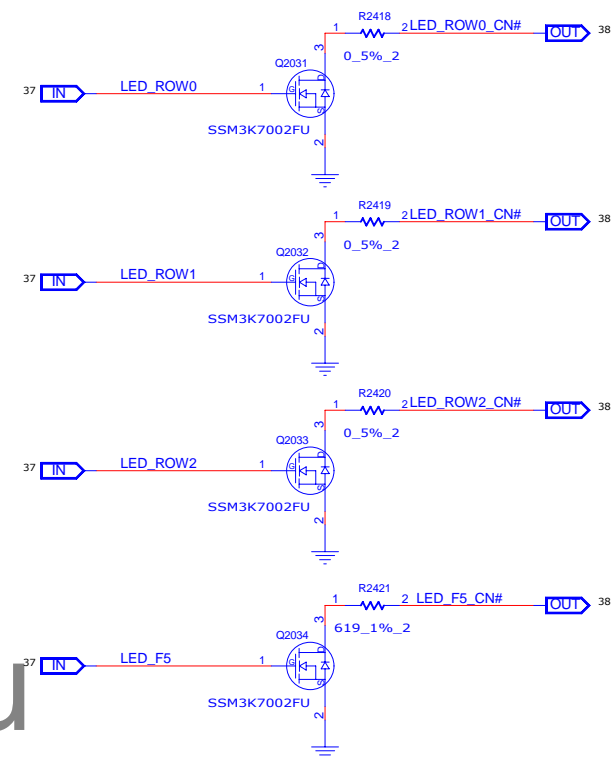
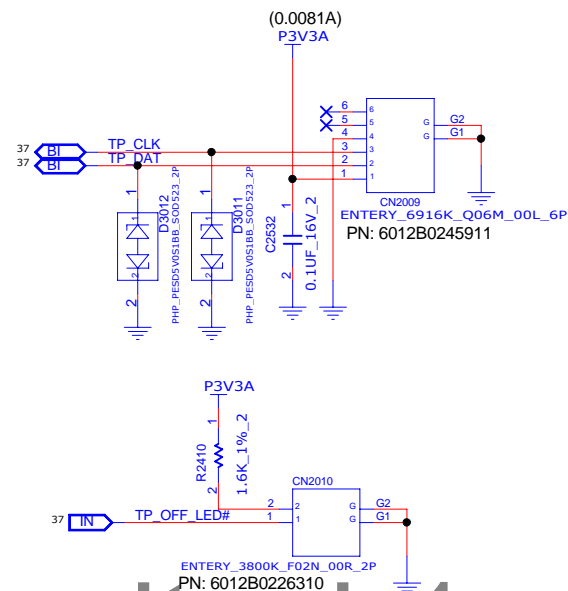
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MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
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DC-JACK LED

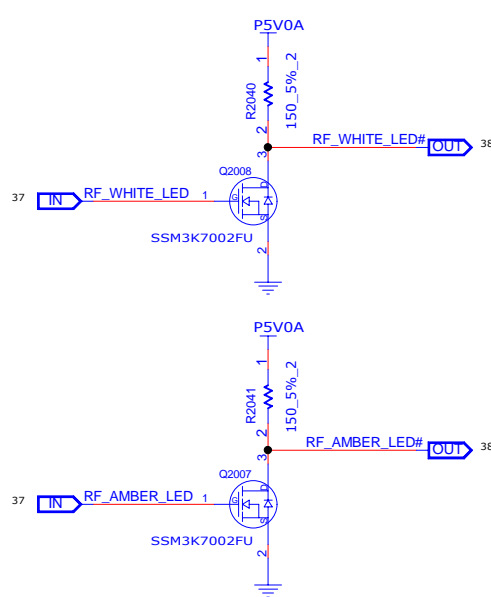
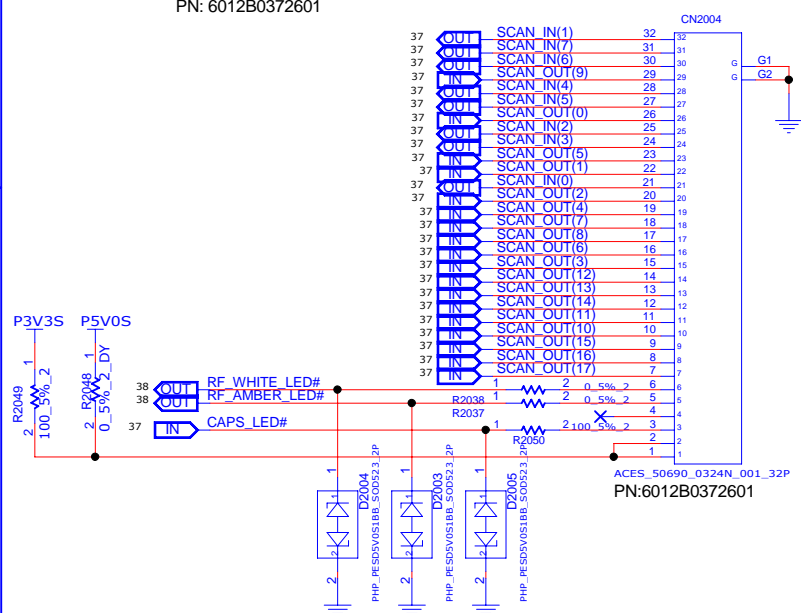


TOUCHPAD MODULE CONN

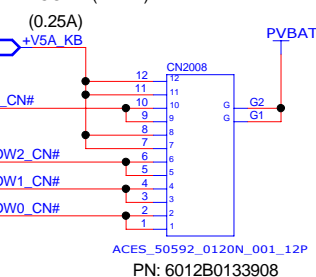


KEYBOARD CONN (32 PIN)

PN: 6012B0372601



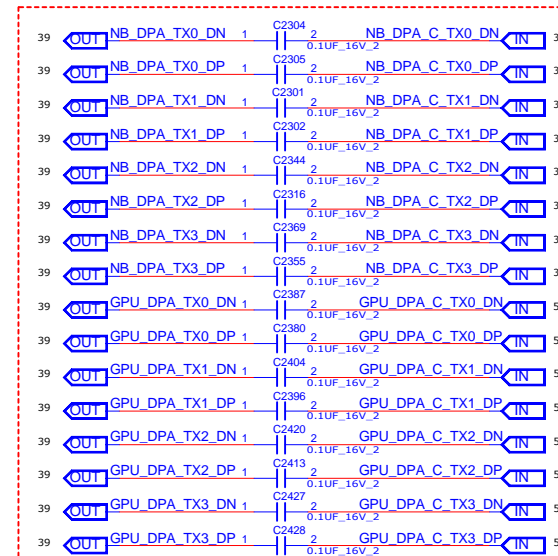
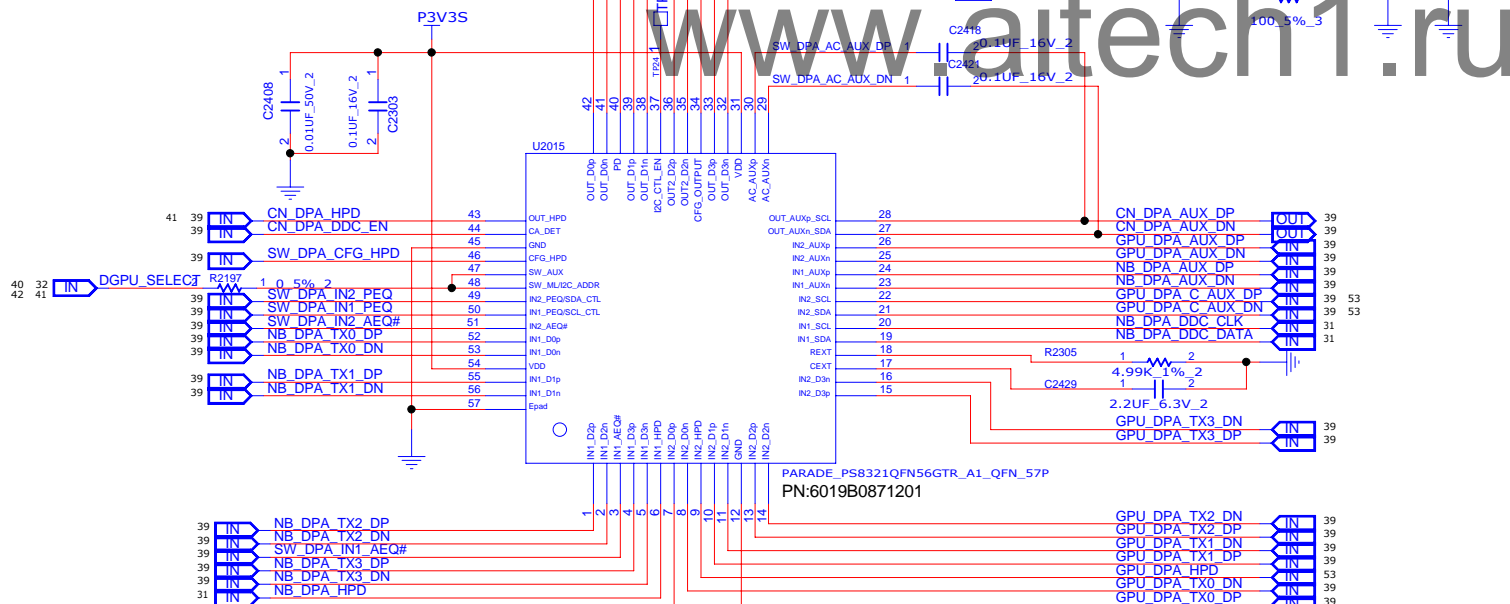
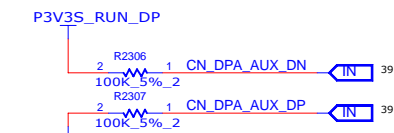
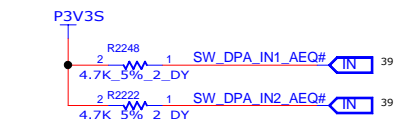
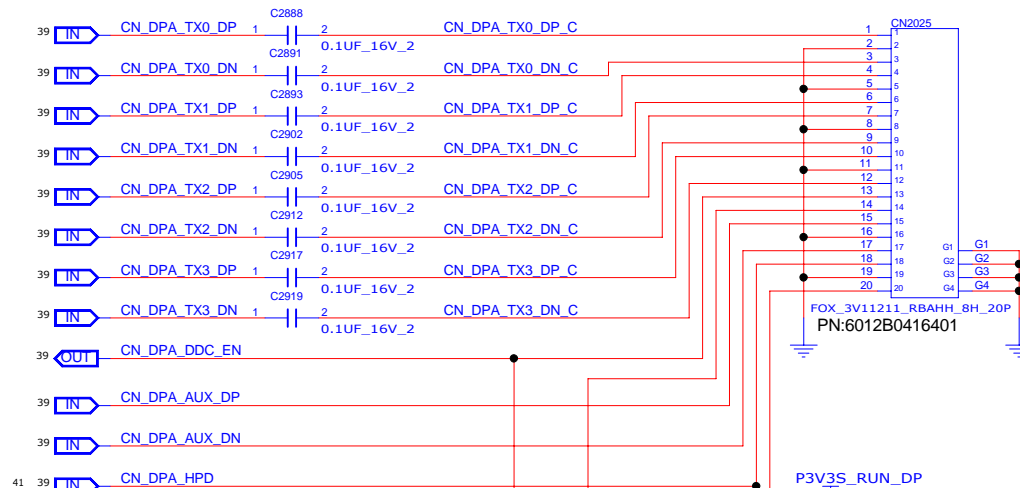
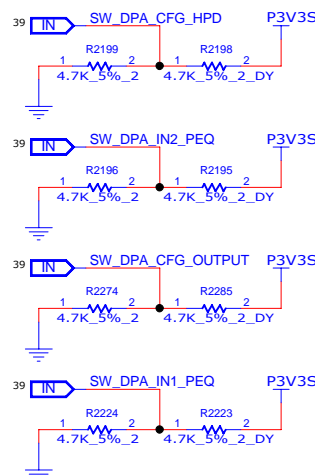
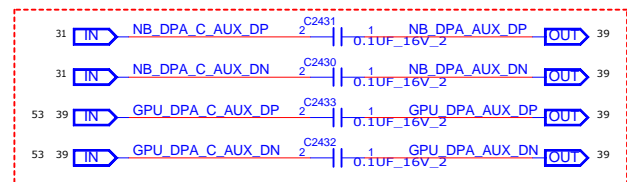
BACK LIGHT LED CONN (12PIN)



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

Display Port A



DGPU_SELECT
H : IN2 PORT IS SELECTED (GPU)
L : IN1 PORT IS SELECTED (NB)

SW_ML=L, PORT1
SW_AUX=L, PORT1
SW_ML=H, PORT2
SW_AUX=H, PORT2

CA_DET=L, AUX
CA_DET=H, I2C

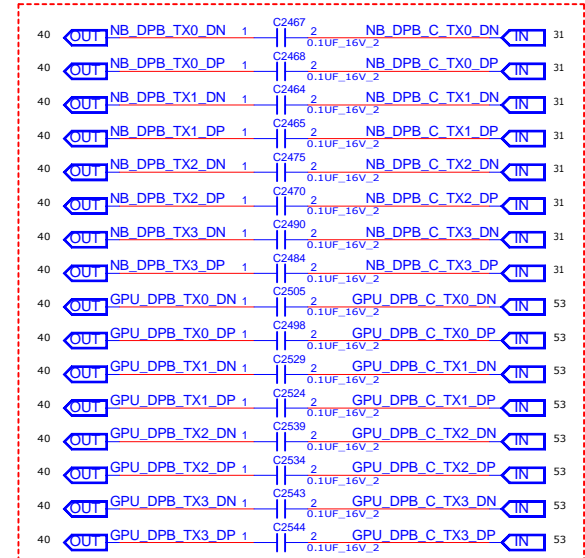
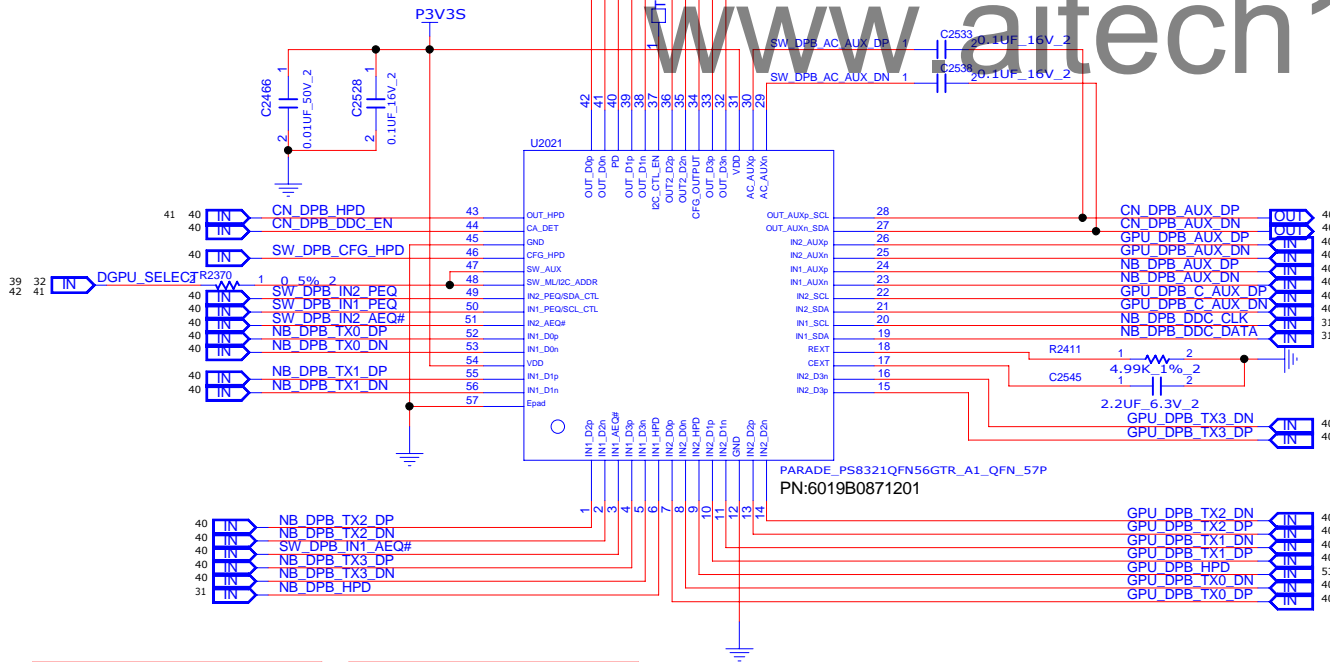
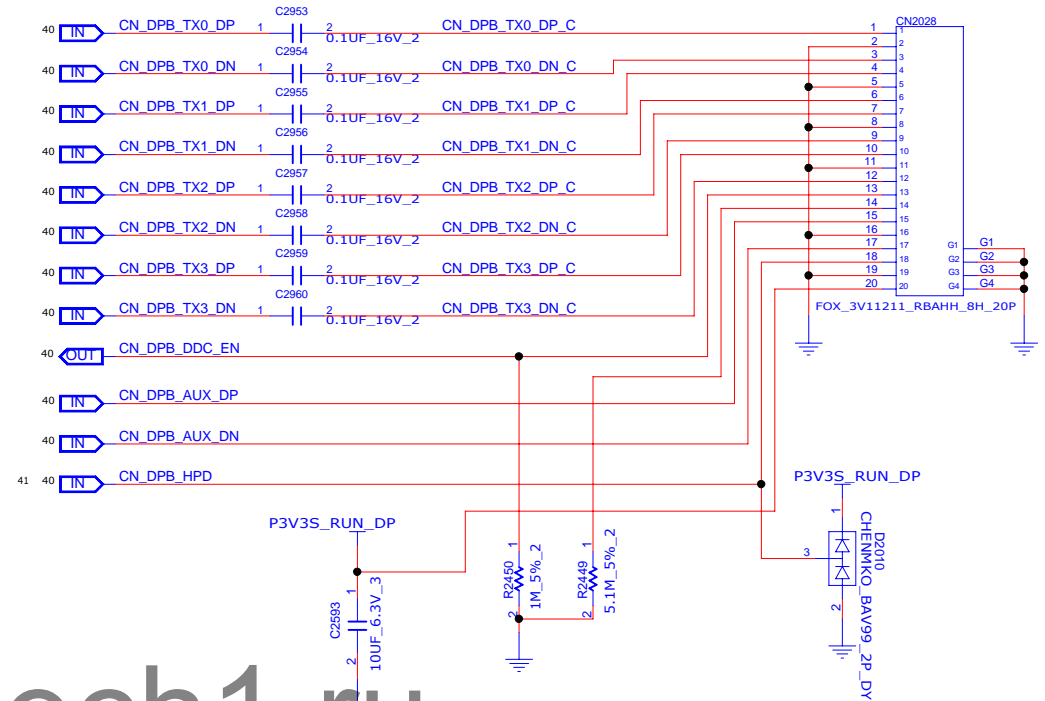
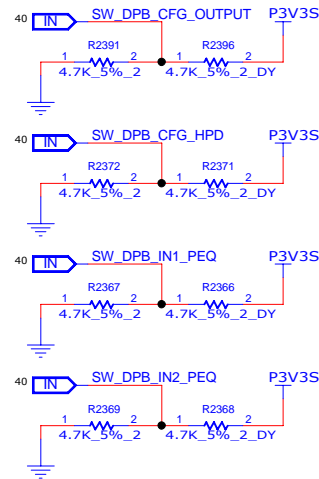
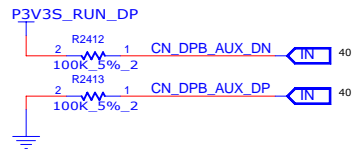
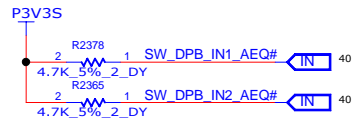
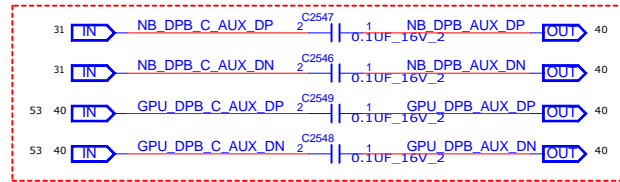
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
DOC NUMBER
1310xxxxx-0-0
REV
X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 39 of 61

Display Port B



DGPU_SELECT
H : IN2 PORT IS SELECTED (GPU)
L : IN1 PORT IS SELECTED (NB)

SW_ML=L , PORT1	CA_DET=L, AUX
SW_AUX=L , PORT1	CA_DET=H, I2C
SW_ML=H , PORT2	
SW_AUX=H , PORT2	

INVENTEC

TITLE	MODEL.PROJECT.FUNCTION

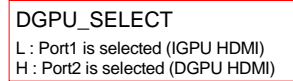
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SIZE A3	CODE CS	1310xxxxx-0-0	X01
SHEET 40 of 61			

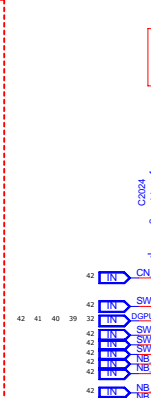
CHANGE by	XXX	DATE	21-OCT-2002
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SHEET 40 of 61

SW_HDMI_DDCBUS IN 41
CN_HDMI_HPB IN 41
CN_HDMI_DDCCLK IN 41
CN_HDMI_DDCDATA IN 41



TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01

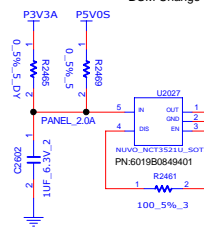
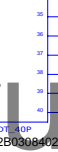


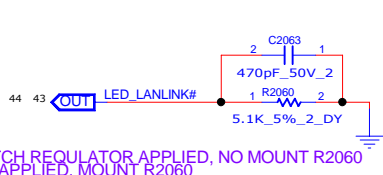
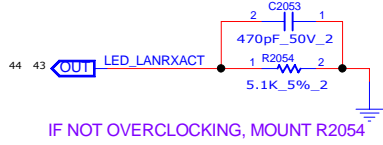
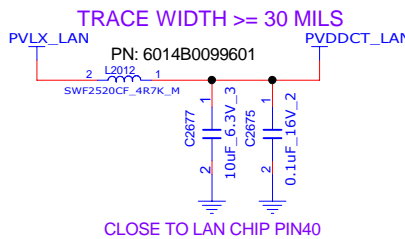
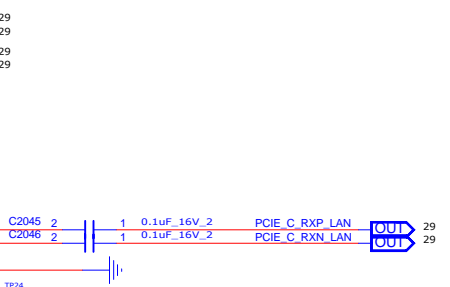
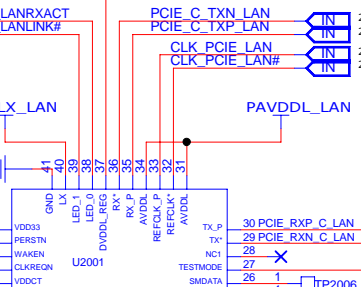
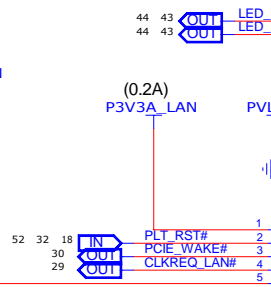
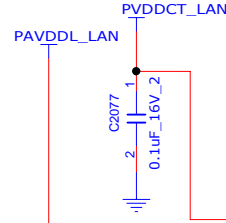
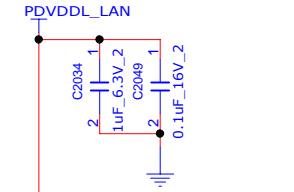
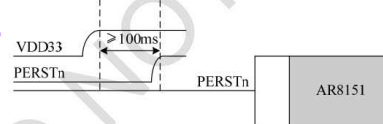
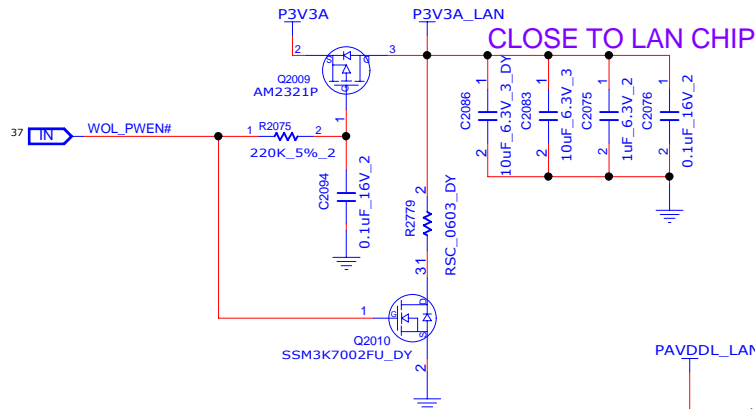
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PN:6019B0491401



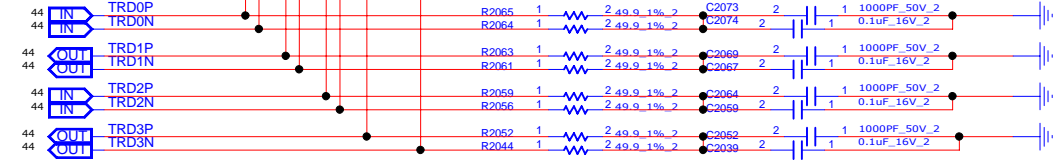
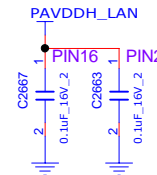
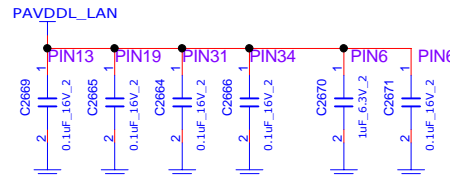
The schematic diagram illustrates the eDP to LVDS interface. It shows the connection of an eDP source to an LVDS sink. The eDP source has pins for CN EDP_AUX_DN, CN EDP_AUX_DP, NB_LCM_DAT, and NB_LCM_CLK. The LVDS sink has pins for MOUNT Ra, Rb, MOUNT Rc, Rd, and OPEN Ra, Rb. The schematic includes resistors (Ra, Rb, Rc, Rd) and a capacitor (C2003) connected to the eDP source pins.

eDP		LVDS	
MOUNT Ra, Rb		MOUNT Rc, Rd	
		OPEN Ra, Rb	





IF SWITCH REGULATOR APPLIED, NO MOUNT R2060
IF LDO APPLIED, MOUNT R2060



INVENTEC

TITLE			
MODEL PROJECT, FUNCTION			
LAN CHIP			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

2D/3D BOM Change

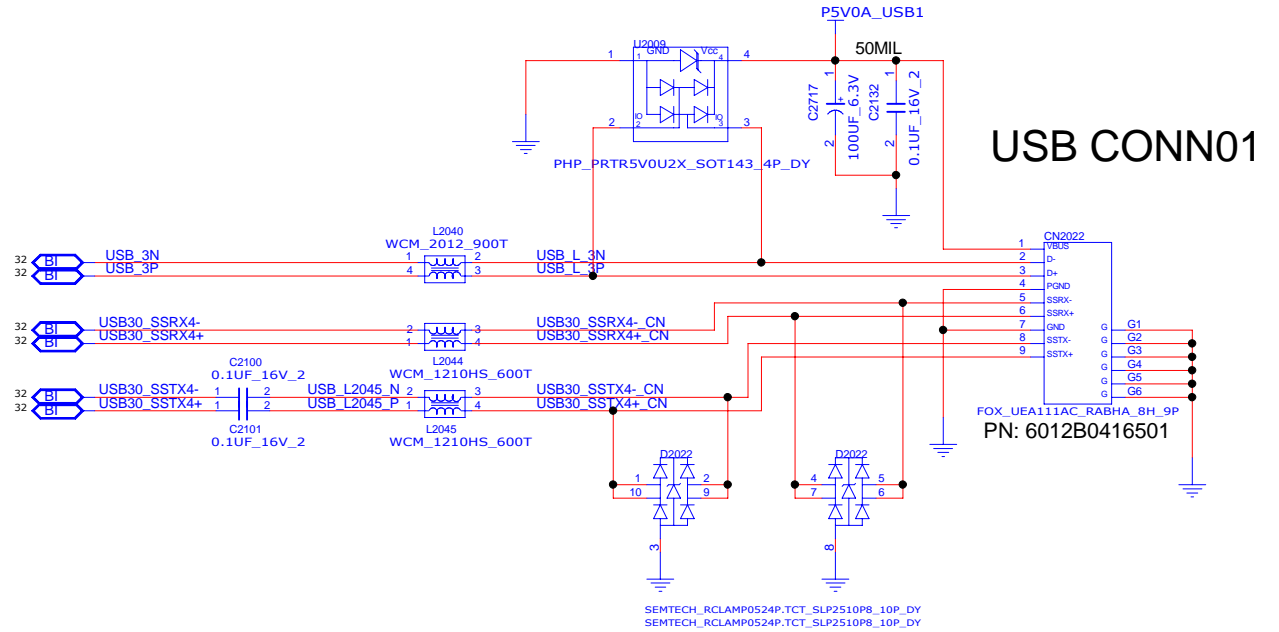
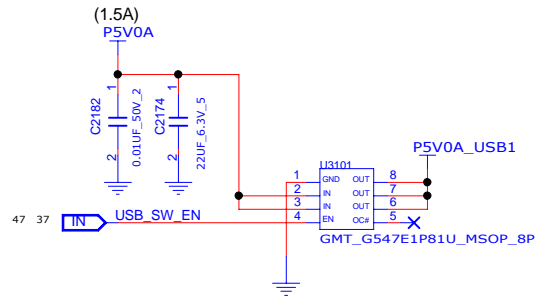


SIZE A3	CODE C5	DOC.NUMBER 1310xxxxx-0-0	FR X
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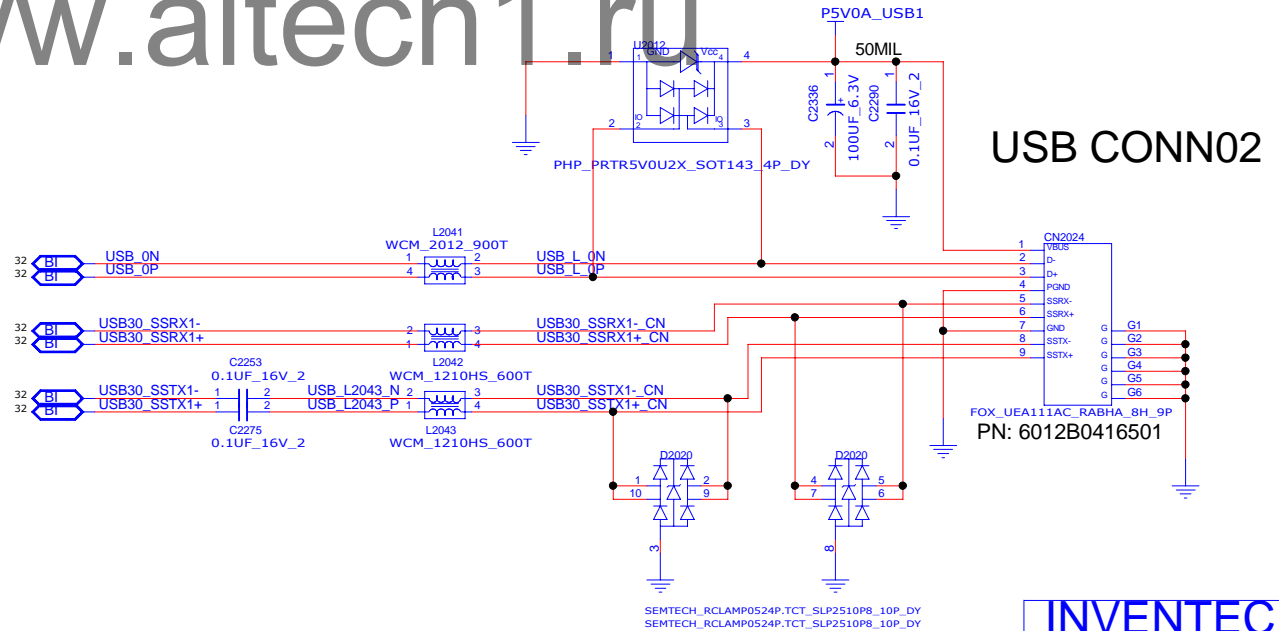
CHANGE by	XXX	DATE	21-OCT-2002
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SHEET 45 of 61

USB3.0



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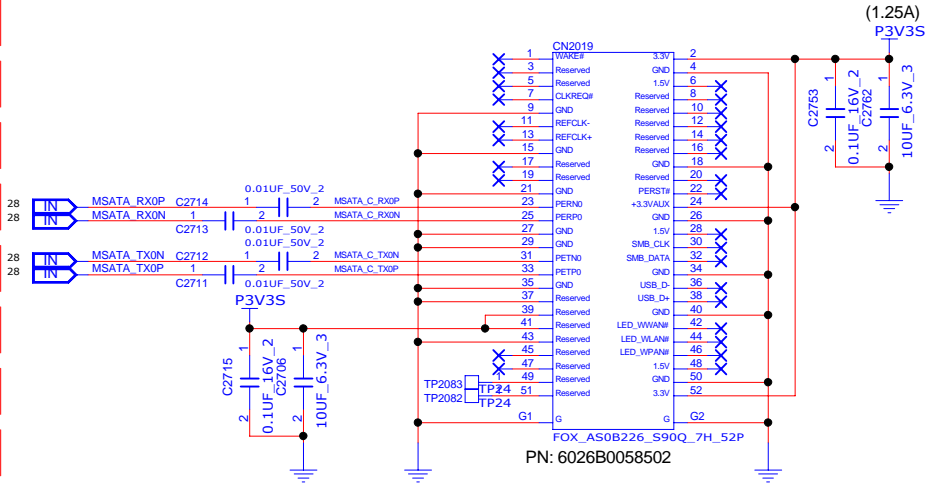
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

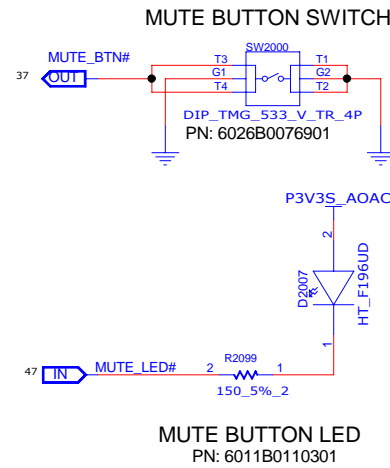
CHANGE by XXX DATE 21-OCT-2002

SHEET 46 of 61

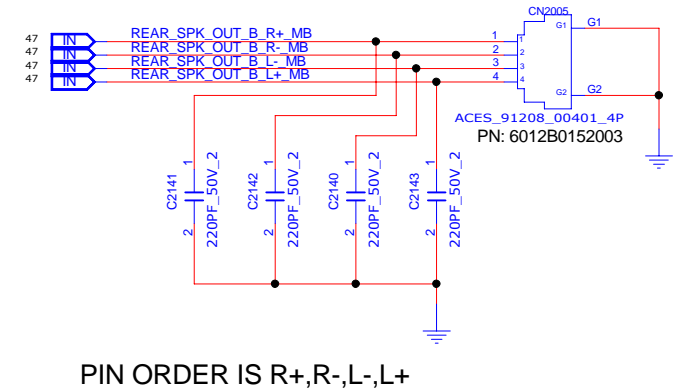
m-SATA BOARD CN ON MB



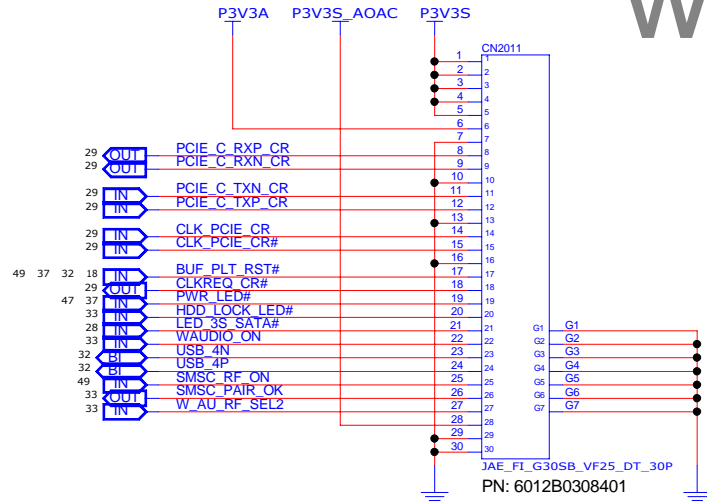
MUTE BOARD CN ON MB



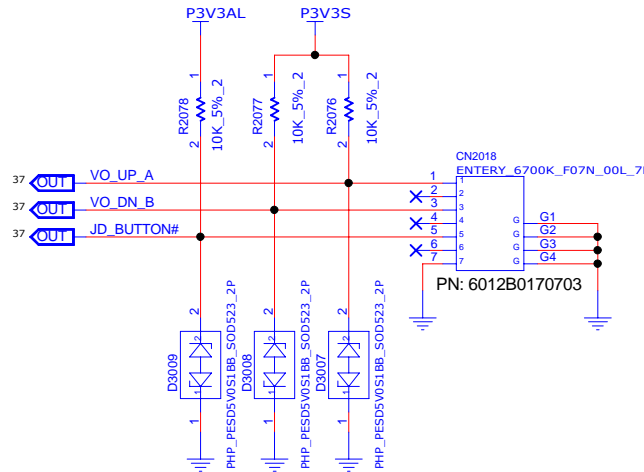
REAR SPEAKER CNTR ON MB



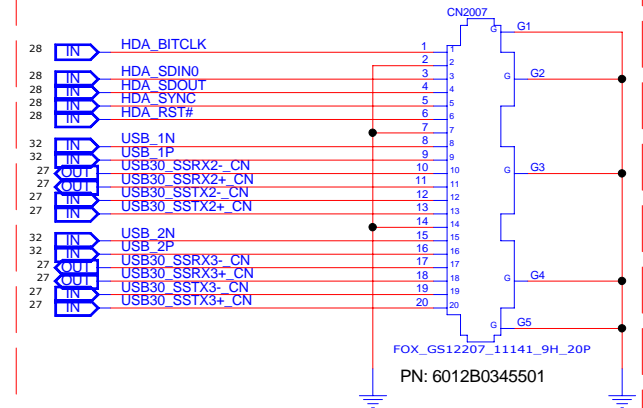
WIRELESS AUDIO COMBO CARD READER CNTR



JOG DIAL CN ON MB JOG DIAL CNTR



AU-USB30 CN ON MB (WIRE OR COXIAL)

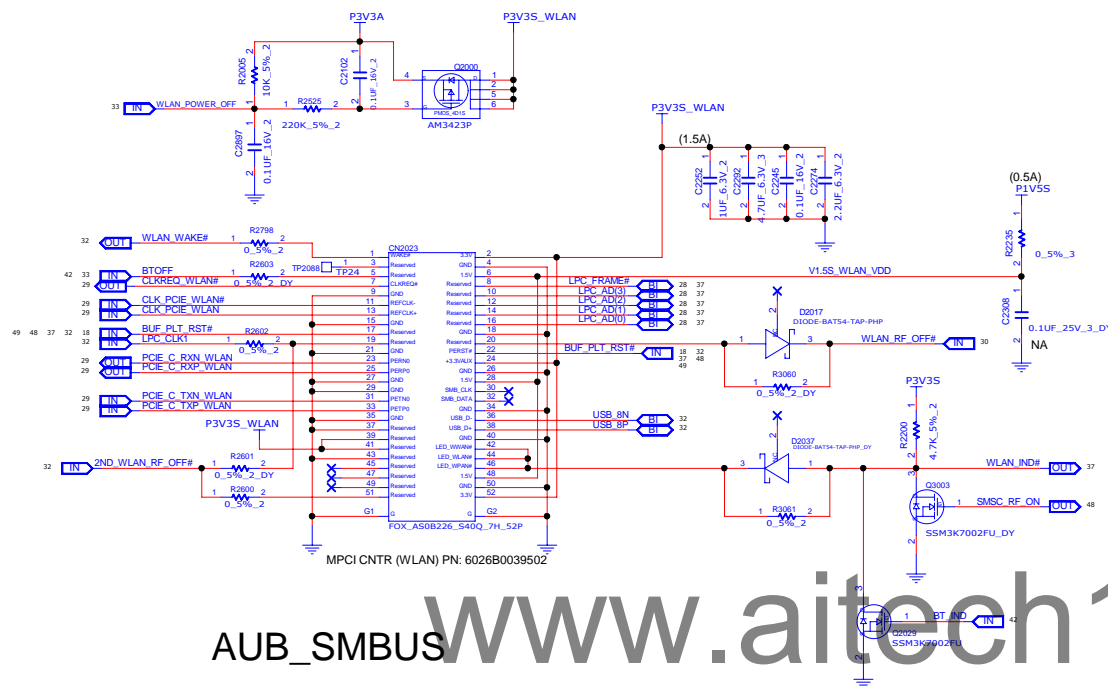


WIRELESS AUDIO COMBO

INVENTEC

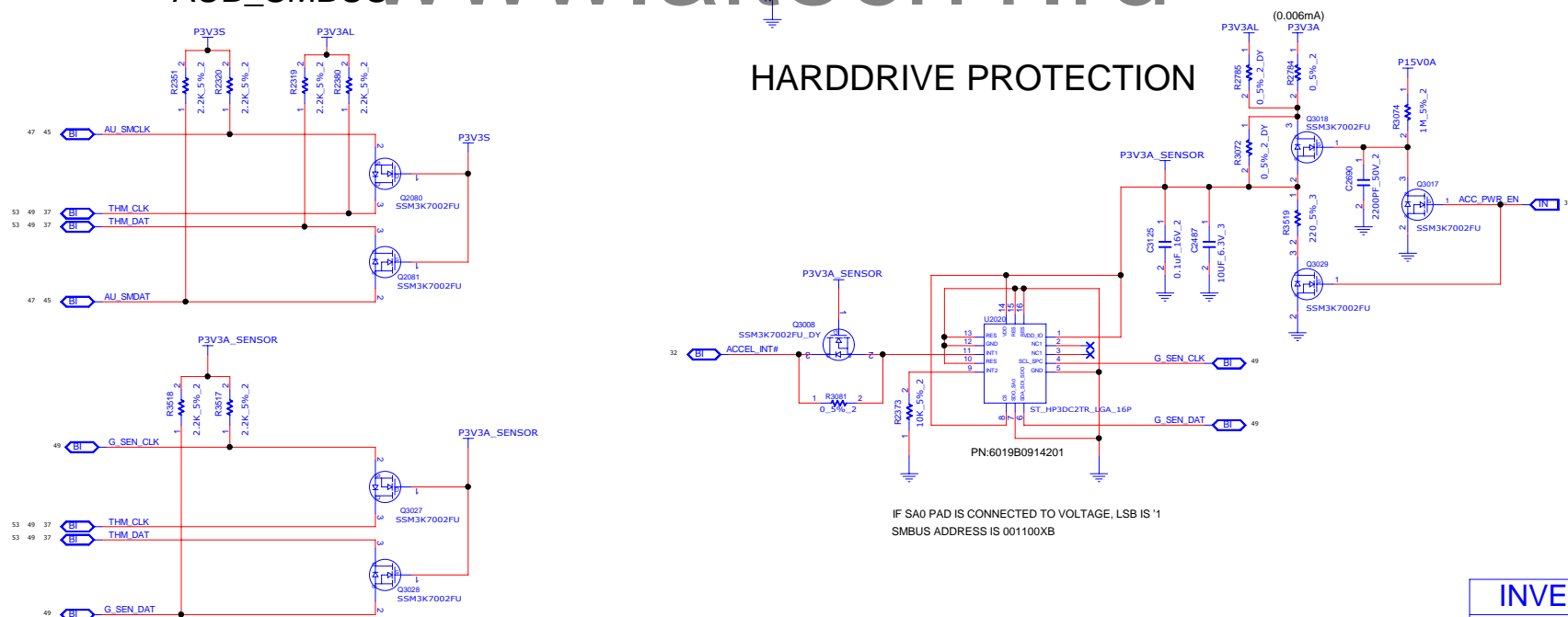
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

WLAN CONN (MINICARD)



	PIN 5	PIN 19	PIN 51
ATHEROS			V (RESERVED)
BROADCOM	V (RESERVED)		
RALINK	V (RESERVED)		
REALTEK	V (RESERVED)		
INTEL (RAINBOW PEAK)		V (ES2 SAMPLE / WW27)	V (QS SAMPLE/WW42)

HARDDRIVE PROTECTION



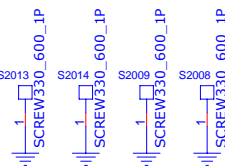
IF SA0 PAD IS CONNECTED TO VOLTAGE, LSB IS '1'
SMBUS ADDRESS IS 001100XB

INVENTEC

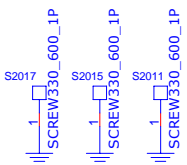
TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxxx-0-0	X01
SHEET 49 of 51			

EMI CAP.

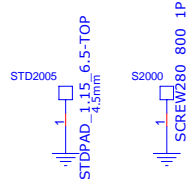
CPU screws



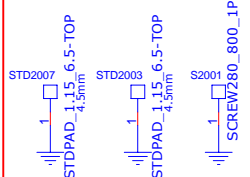
VGA screws



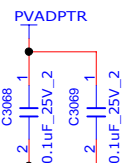
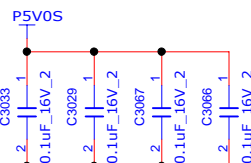
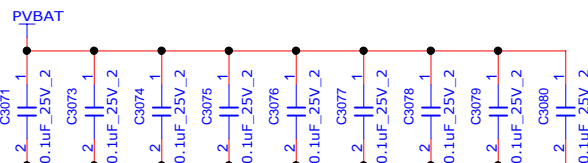
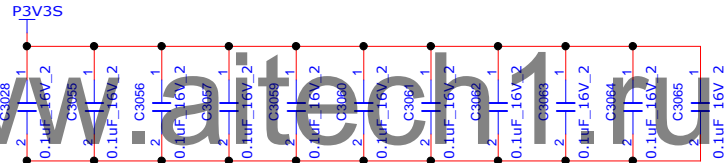
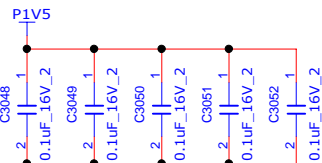
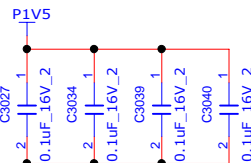
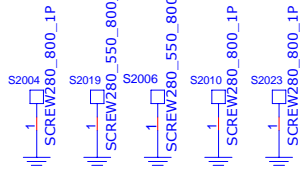
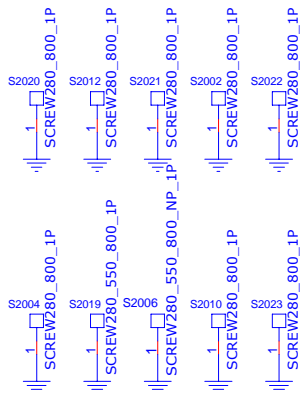
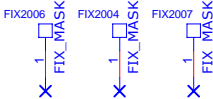
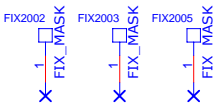
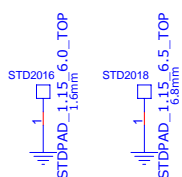
DGPU FAN screws



IGPU FAN screws



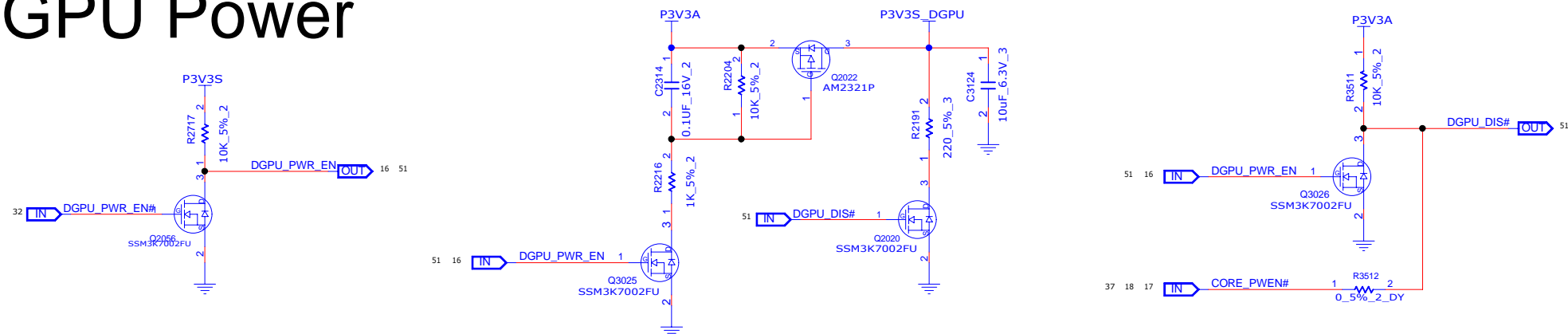
WLAN screws



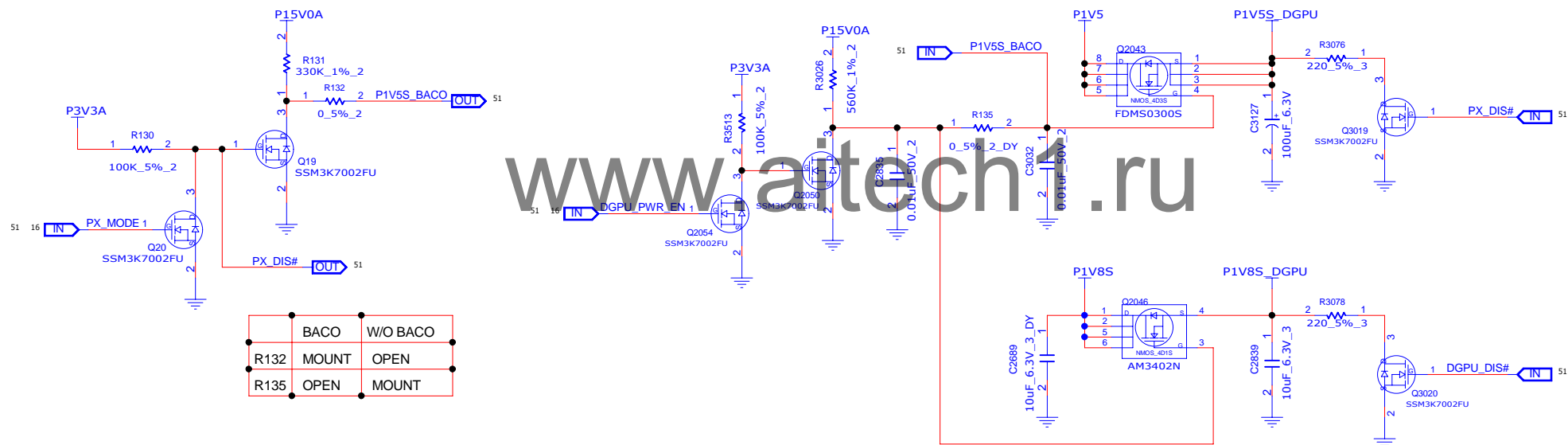
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

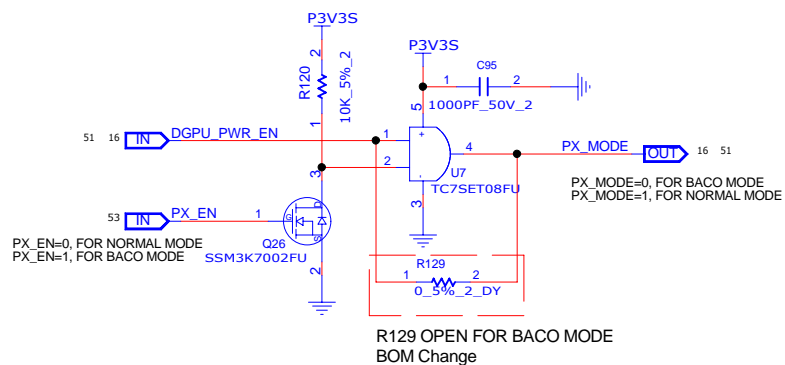
A



MOUNT FOR BACO MODE



	BACO	W/O BACO
R132	MOUNT	OPEN
R135	OPEN	MOUNT



R129 OPEN FOR BACO MODE
BOM Change

INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
Block	Diagram

SIZE A3	CODE C5	DOC.NUMBER 1310xxxxx-0-0	R X
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CHANGE by	XXX	DATE	21-OCT-2002
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SHEET 51 of 61

8	7	6	5	4	3	2	1
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AMD(Heathrow Pro)

PN:6019B0936101

BOM Change

U2044

PART 1 OF 9

PCI EXPRESS INTERFACE

AMD_216_0834002_00_FCBGA_962P

P3V3S_DGPU

C2313

0.1UF_16V_2

U2013

TC7SZ08FU

100K_5%_2

PEG_PLT_RST#

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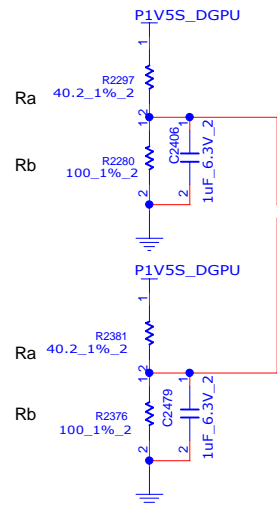
282

283

CHANNEL A

DDR3/GDDR3 MEMORY STUFF OPTION

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



FOR M97,BROADWAY,MADISO AND PARK ONLY

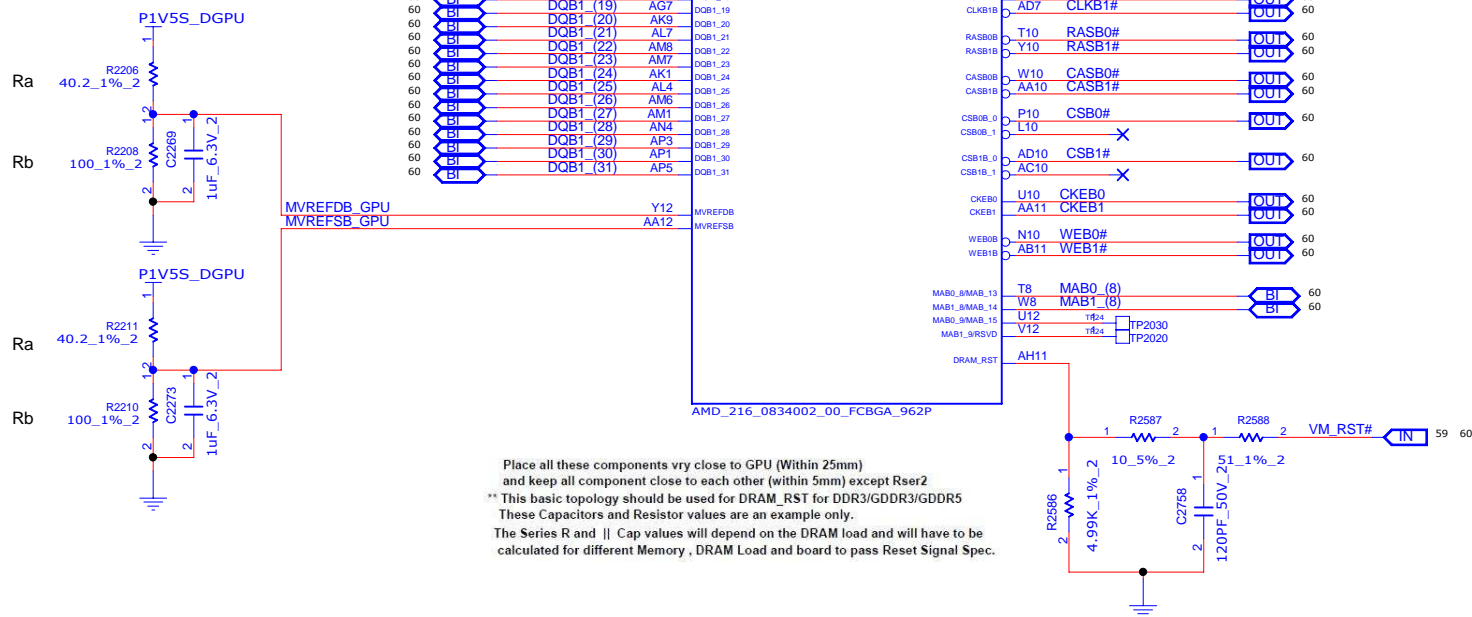
U2044

PART 3 OF 9
GDDR5/DDR3

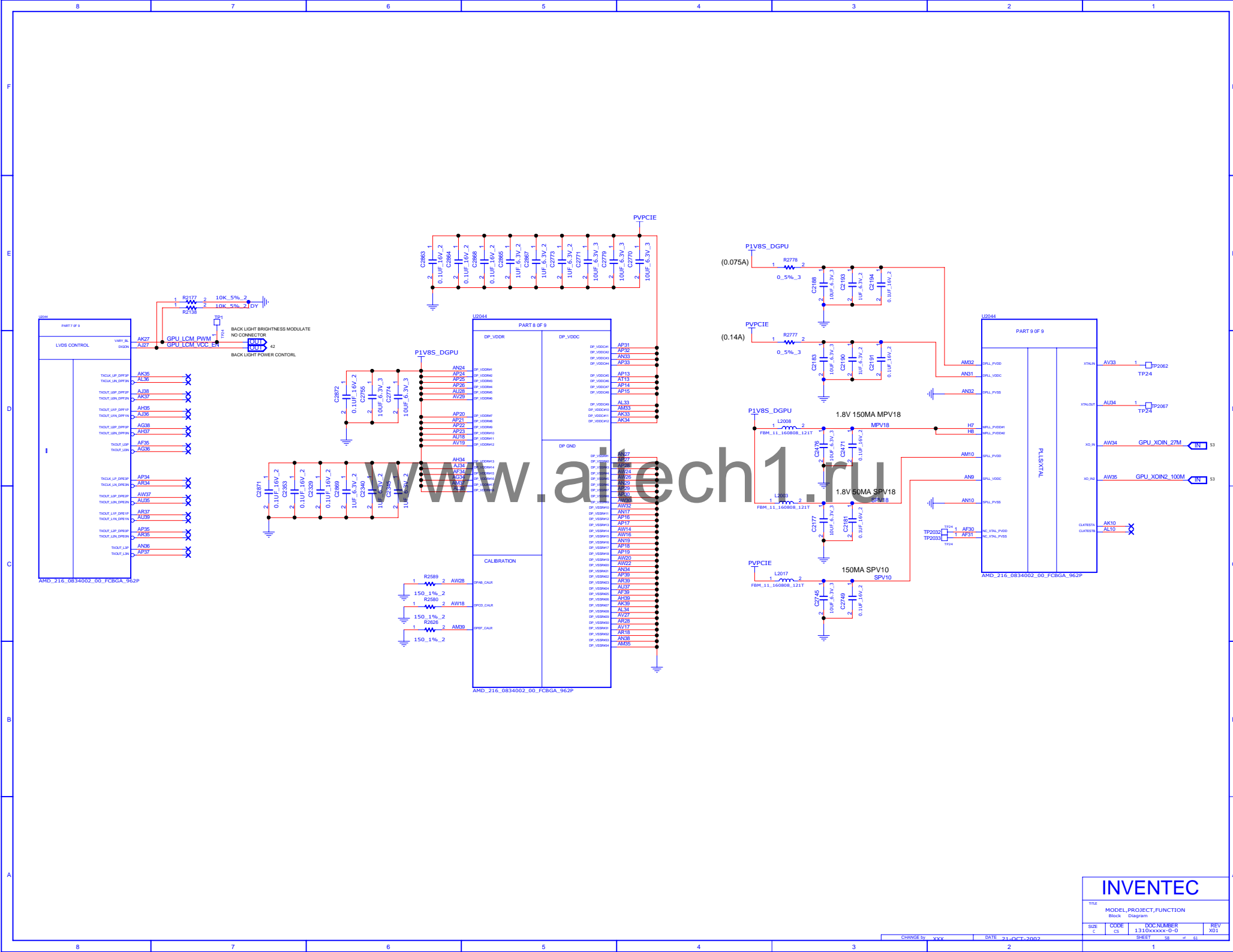
MEMORY INTERFACE



SHEET 55 of 61



AMD 216 0834002 00 FCBGA 962P



SAMSUNG P/N = 6019B0660401
HYNIX P/N = 6019B
CIMONDA P/N =

CHANNEL B MEMORY



P1VSS_DGPU

P1VSS_DGPU

P1VSS_DGPU

P1VSS_DGPU

P1VSS_DGPU

P1VSS_DGPU

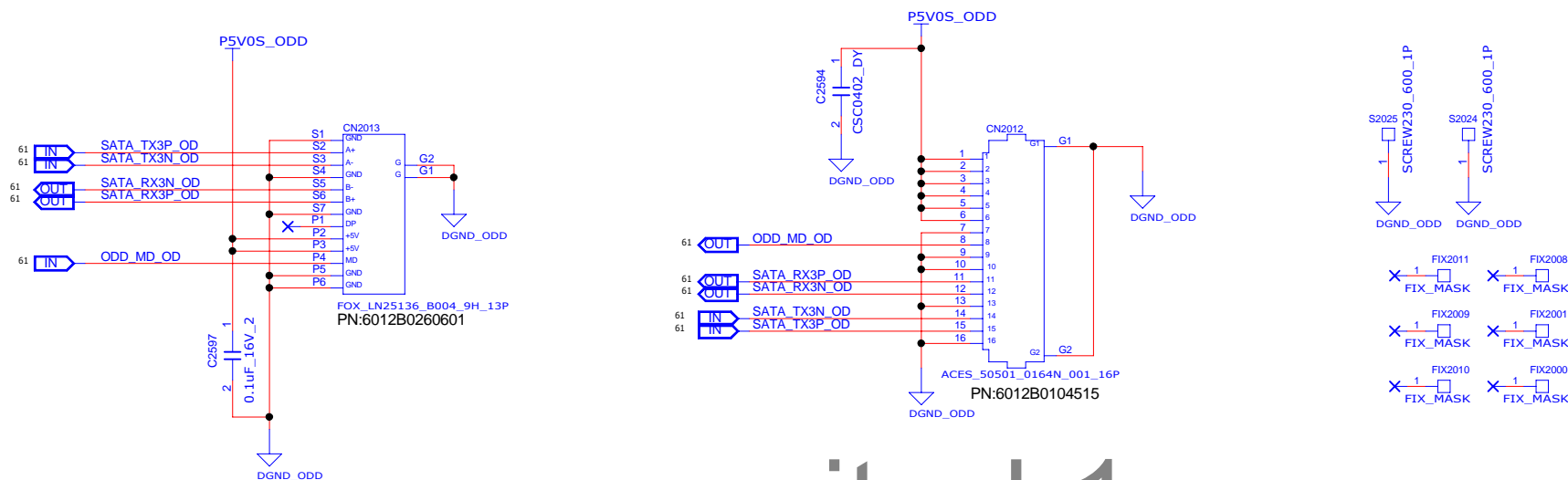
MF = 1 FOR MIRROR

INVENTEC

MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310XAXX-0-0	X01
SHEET		60	61

CHANGE BY: YXX DATE: 21-OCT-2002

ODD Board: 6050A2490701



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INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

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